



H55H-CM

V : 1.0


SCHEMATICS TABLE:

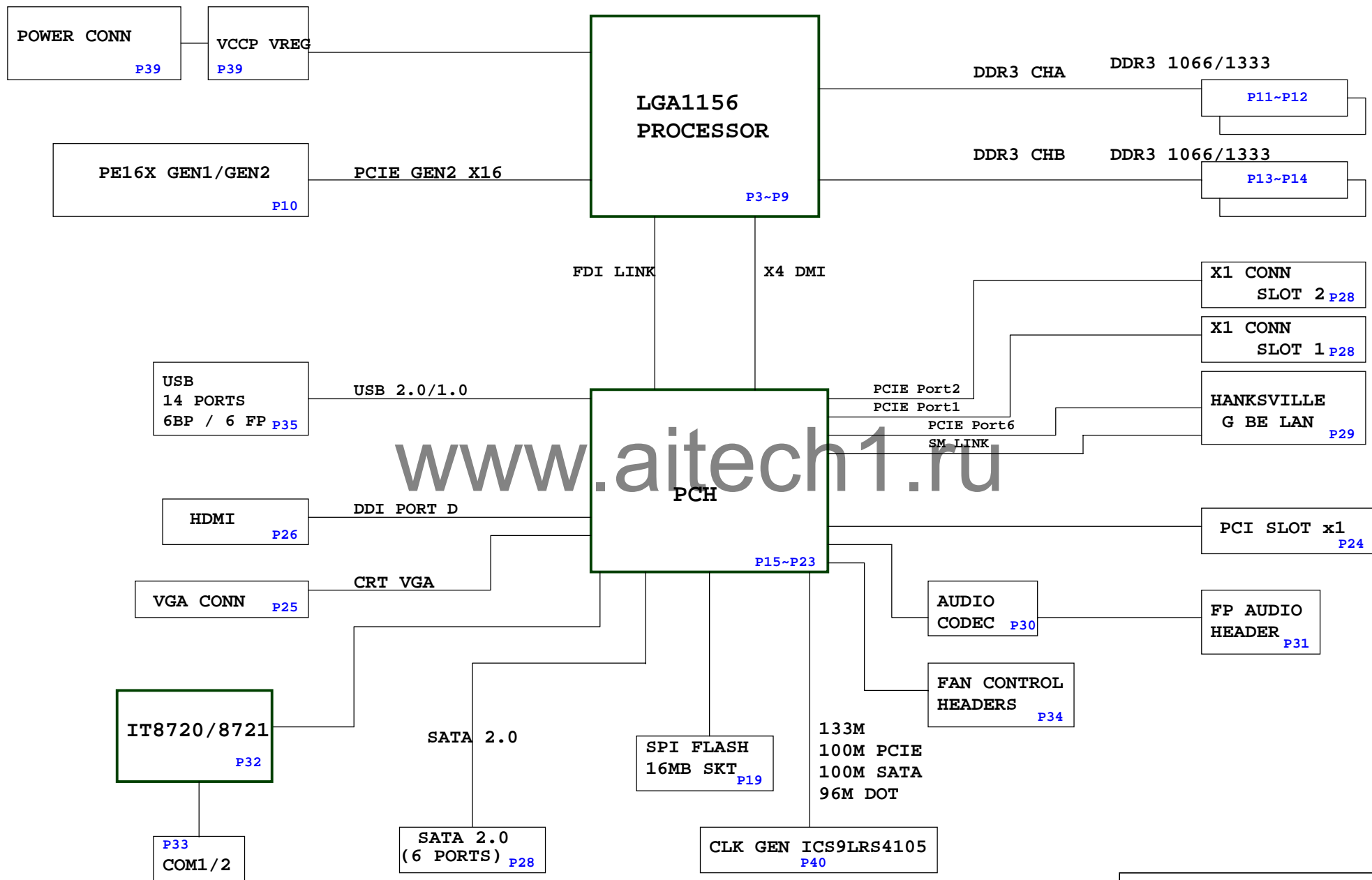
Page	Index	Page	Index
1	COVER PAGE	24	PCI
2	Block Diagram	25	VGA Connector
3	CPU MISC&Flexible Display Interface	26	HDMI(Level shifter&Connector)
4	CPU DMI&PEG	27	Primary&PCH XDP
5	CPU DDR3-A	28	SATA&PCI-E X1
6	CPU DDR3-B	29	Hanksville(82578DC)
7	CPU CFG	30	Audio ALC662/ALC888S
8	CPU Power(VCCP,V_AXG,VTT)	31	Audio Connector
9	CPU GND&RSVD	32	IT8720F/8721F
10	PCI-E 16X	33	COM,KBMS,FDD,LPT
11	CONN DDR3 CH A DIMM0	34	F_PANEL&Smart Fan
12	CONN DDR3 CH A DIMM1	35	USB Header&Port
13	CONN DDR3 CH B DIMM0	36	DC-DC CPU_VTT,5VDUAL
14	CONN DDR3 CH B DIMM1	37	DC-DC V_AXG,V_1P05_ME
15	PCH USB&PCIE	38	DC-DC PCH Core,VDIMM,V_1P8_SFR
16	PCH SATA,HOST,CLINK,PCI	39	DC-DC CPU Vcore
17	PCH GPIO,AUDIO,LPC,SPI	40	CLK GEN CK505(ICS9LRS4105)
18	PCH NVRAM	41	Power Delivery
19	PCH FDLINK&SPI ROM&TCM	42	PWRGD&RST Tree
20	PCH PWR RAILS,Decoupling	43	Clock Map
21	PCH GND Pins		
22	PCH Video and DDSP		
23	PCH CLOCKS,Straps		

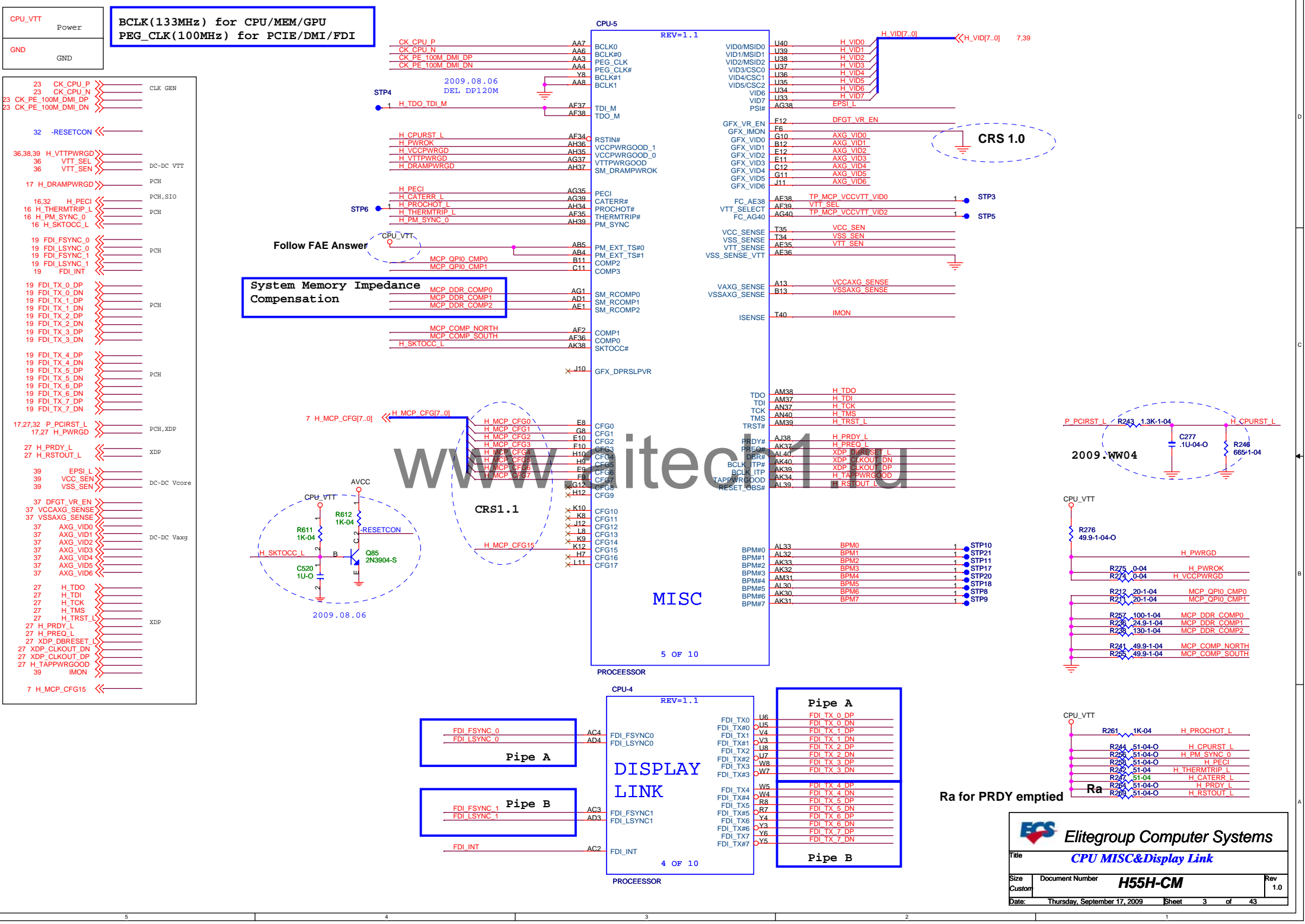
REVISION HISTORY:

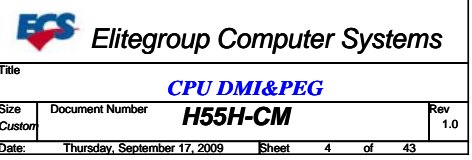
Rev	Date	Notes
V1.0	2009/10/29	1.change model name to H55H-CM 2.change PCH to H55 3.Add HDMI&VGA function

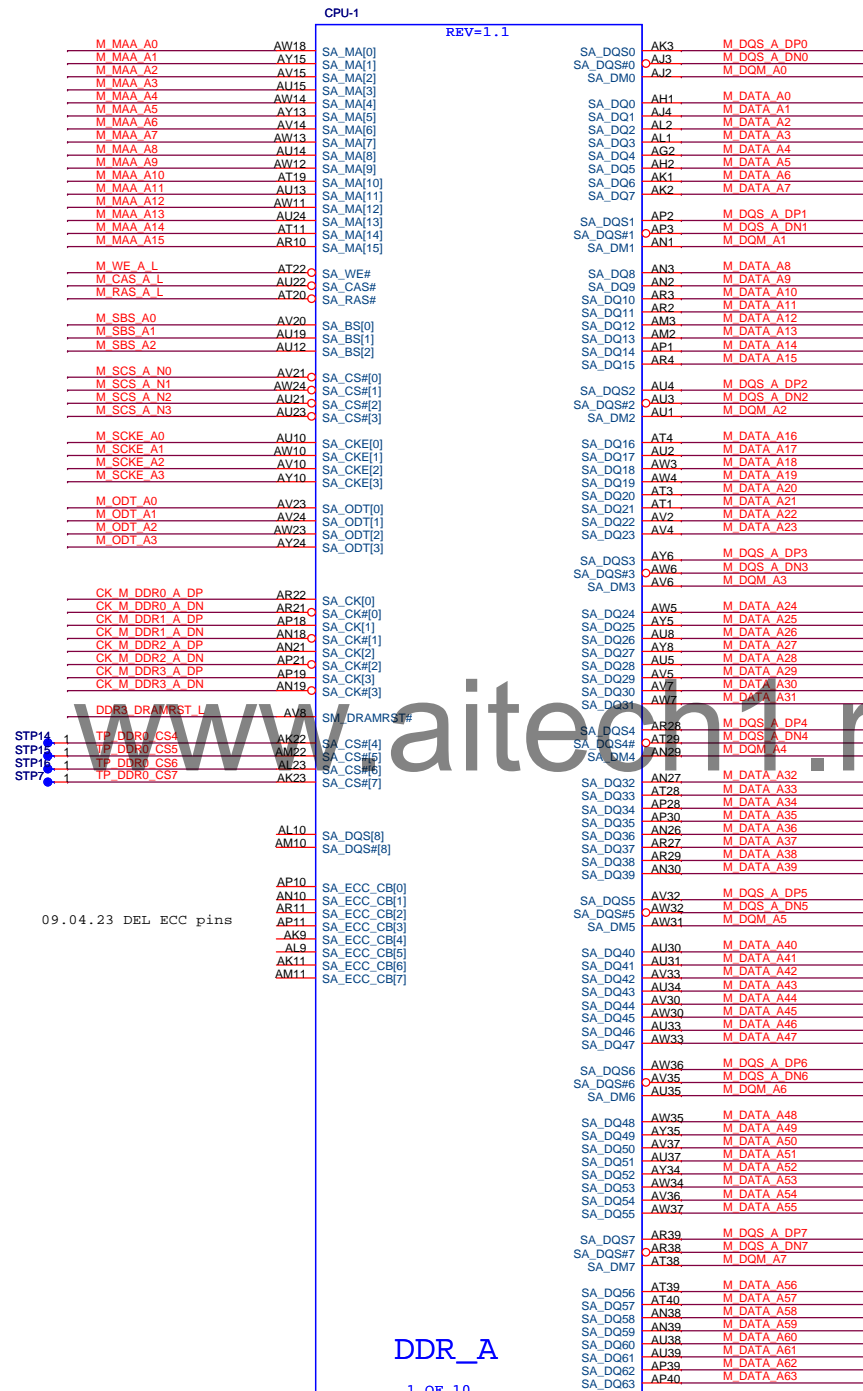
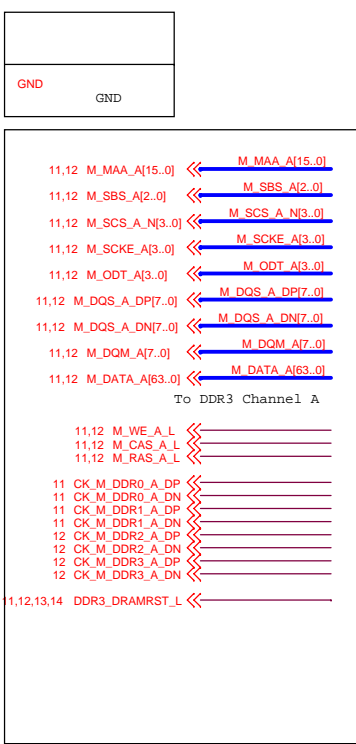
@ ECS CONFIDENTIAL @

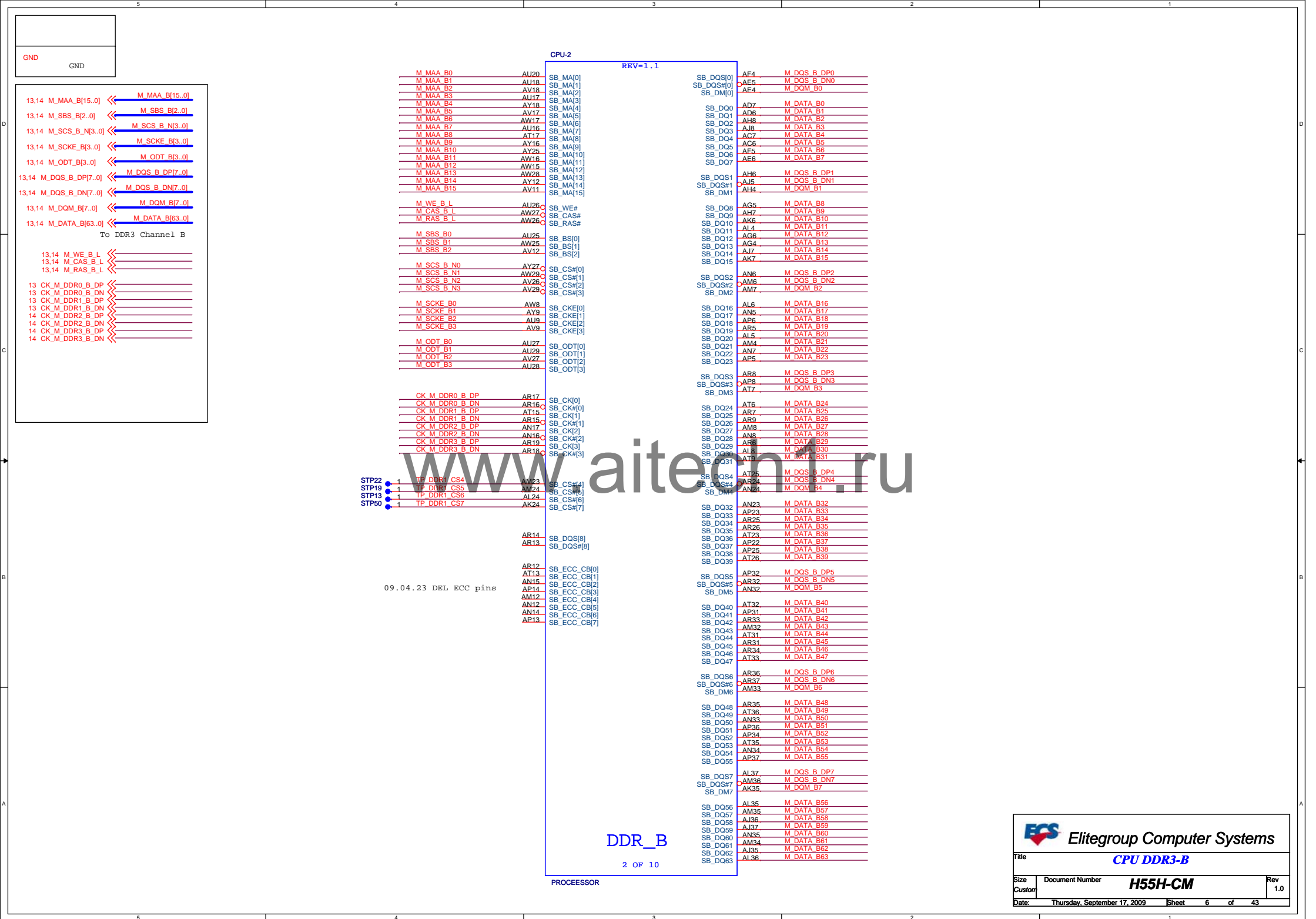
 Elitegroup Computer Systems	
Title Cover Page	
Size Custom	Document Number H55H-CM Rev 1.0
Date: Thursday, October 29, 2009 Sheet 1 of 43	





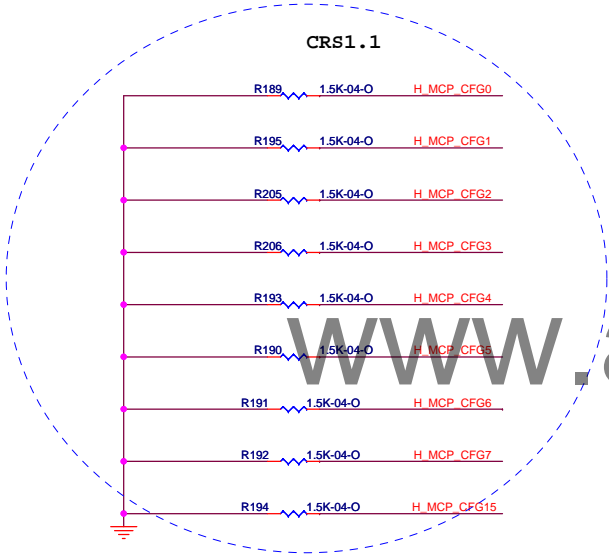




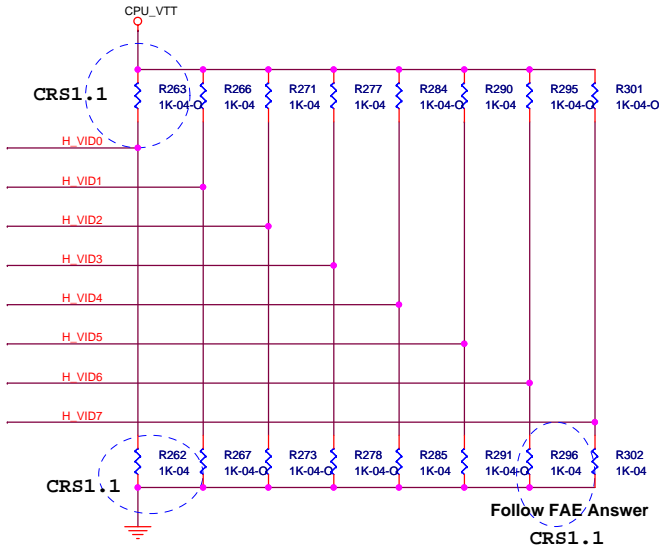


CPU_VTT	Power
GND	GND

3 H_MCP_CFG[7..0]	>> H_MCP_CFG[7..0]	CPU
3 H_MCP_CFG15	>> H_MCP_CFG15	
3.39 H_VID[7..0]	<< H_VID[7..0]	CPU, DC-DC Vcore



CFG	Havendale	Lynnfield	DESCRIPTION
0	1X16	2X8	PEG SEL (1X16, 2X8)
1	RSVD		PEG SEL1
2	RSVD		PEG SEL3
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLED	ENABLED	DP PRESENCE
	RSVD		
6	RSVD		
7	RSVD		ENGINEERING - REMOVE ON PRODUCTION DESIGN
15	RSVD		ENGINEERING - REMOVE ON PRODUCTION DESIGN
CFG 0,1,2,3,4,5,6,7,15 HAVE INTERNAL PULL-UPS			



POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	Icc(MAX)=120A	Icc(MAX)=120A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

Title

CPU CFG

Size

Document Number

H55H-CM

Rev

1.0

Date:

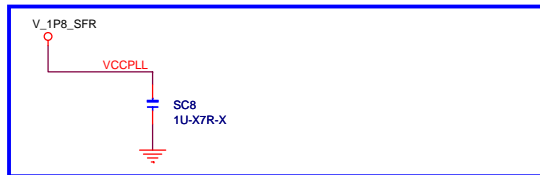
Thursday, September 17, 2009

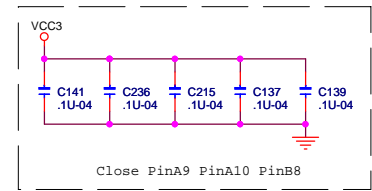
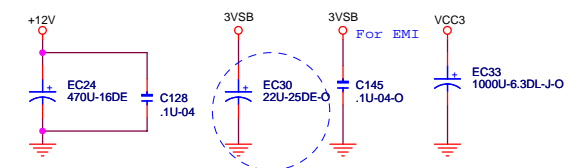
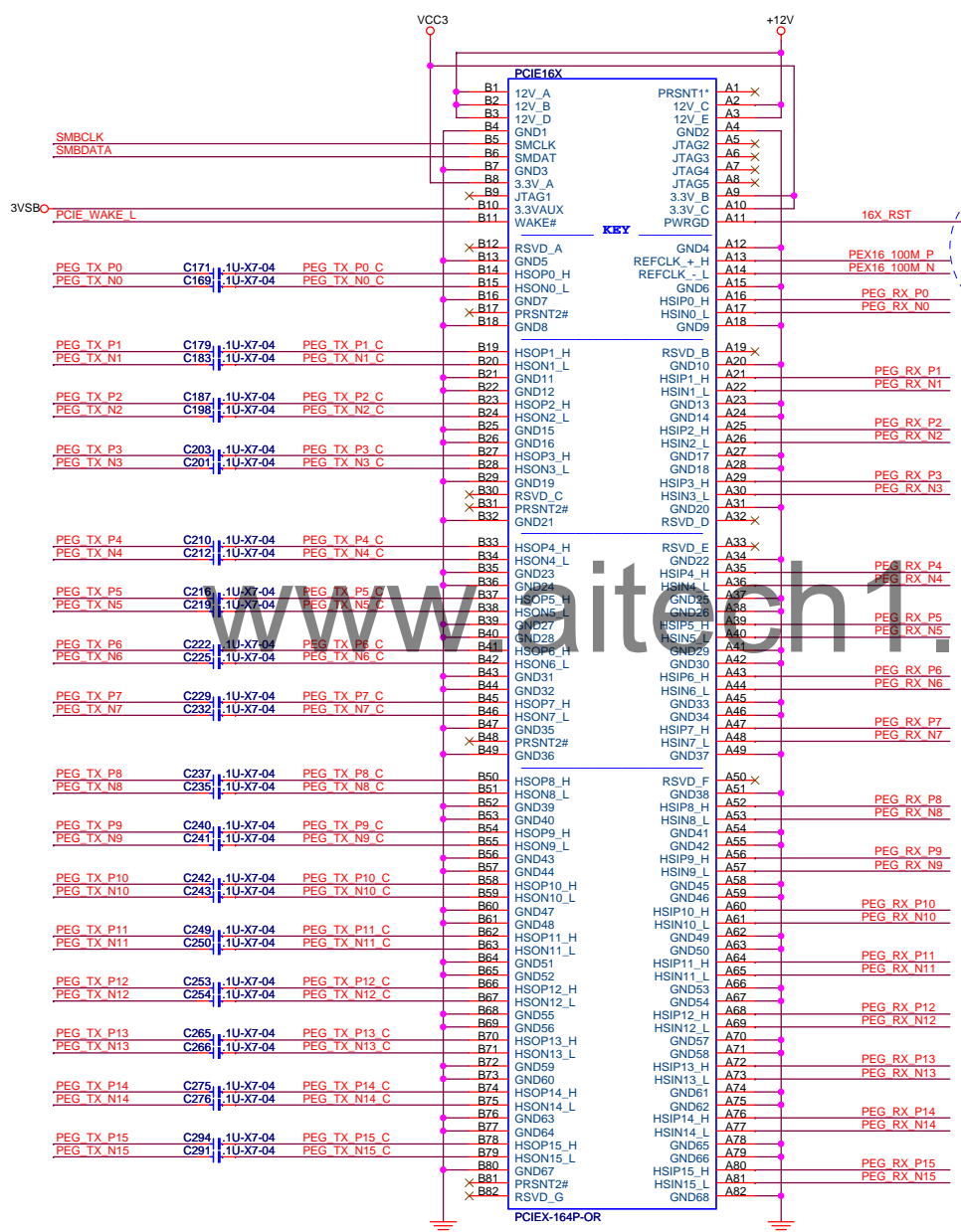
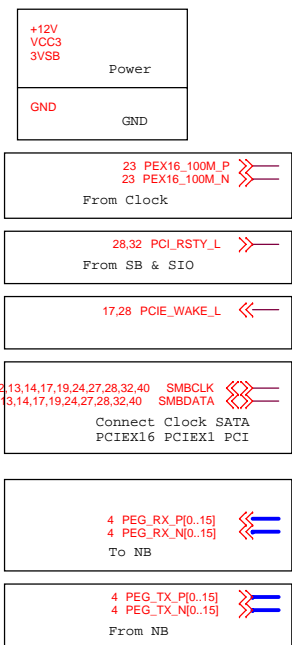
Sheet

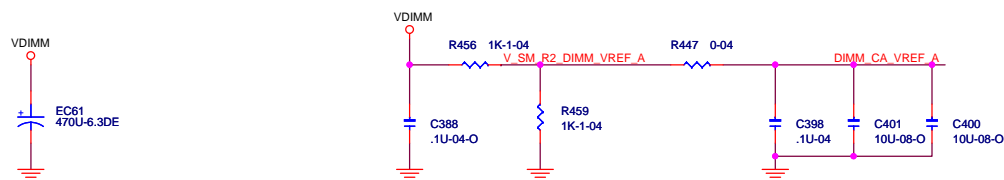
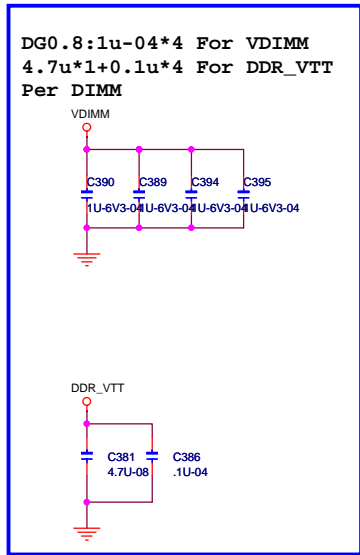
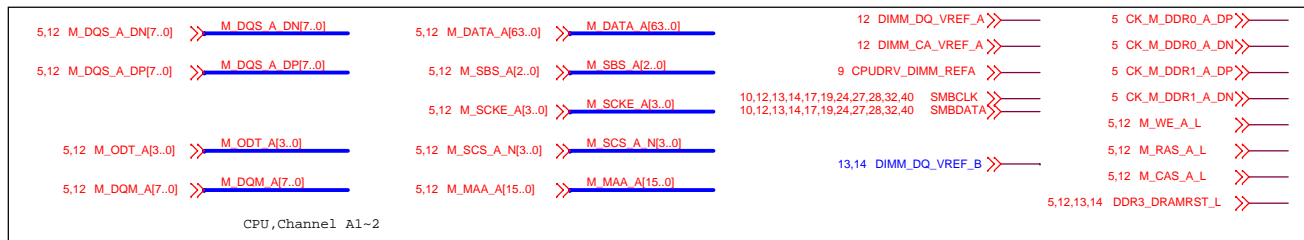
7

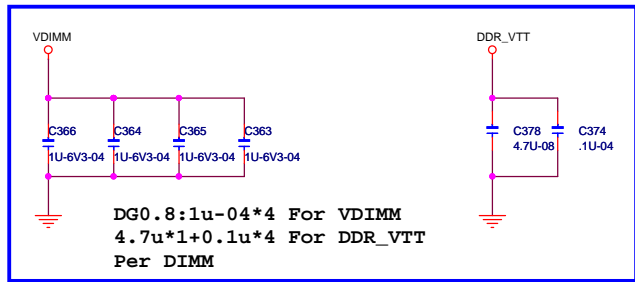
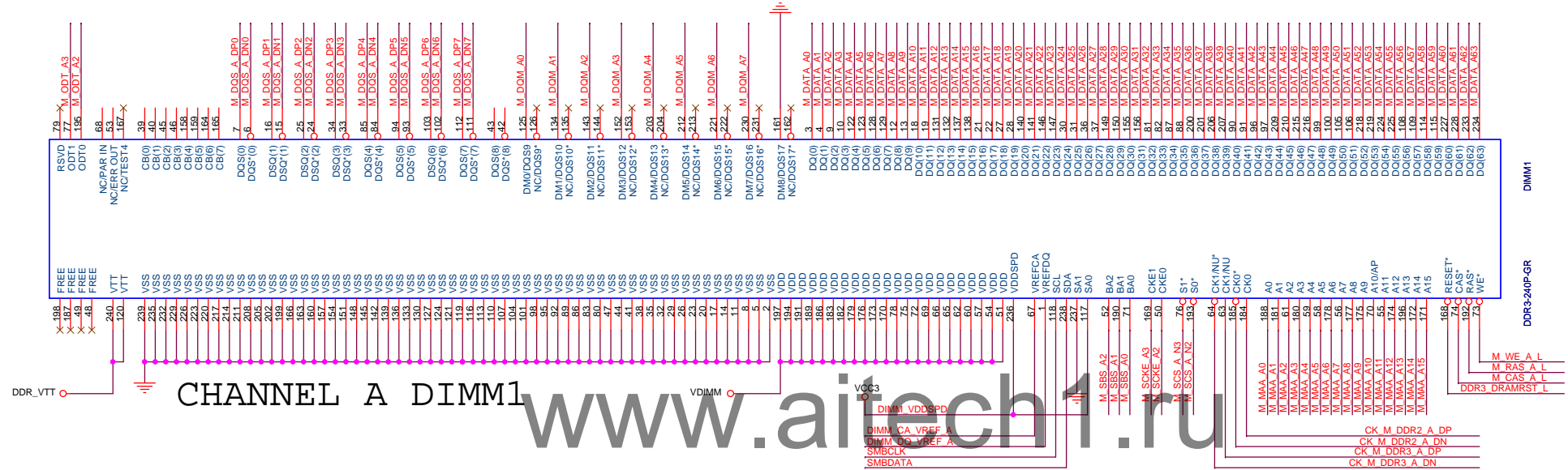
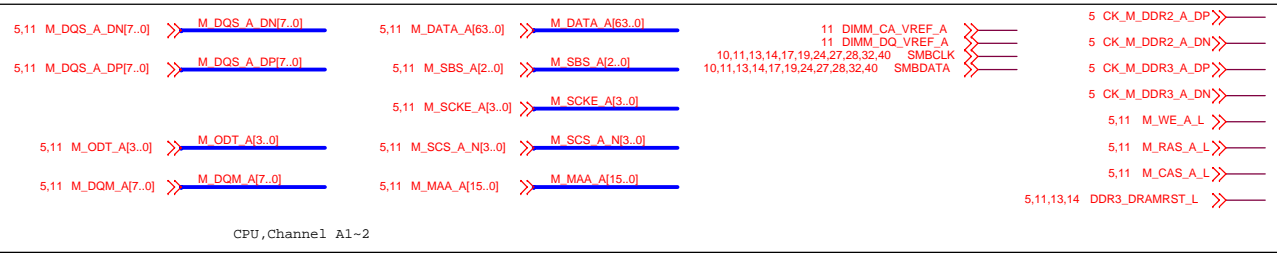
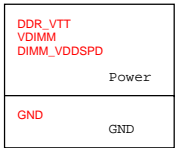
of

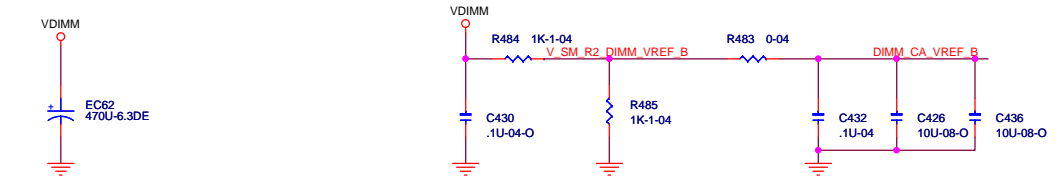
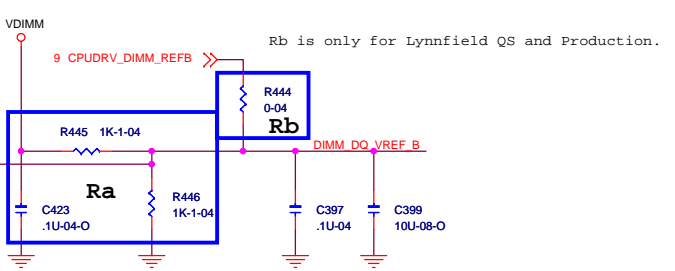
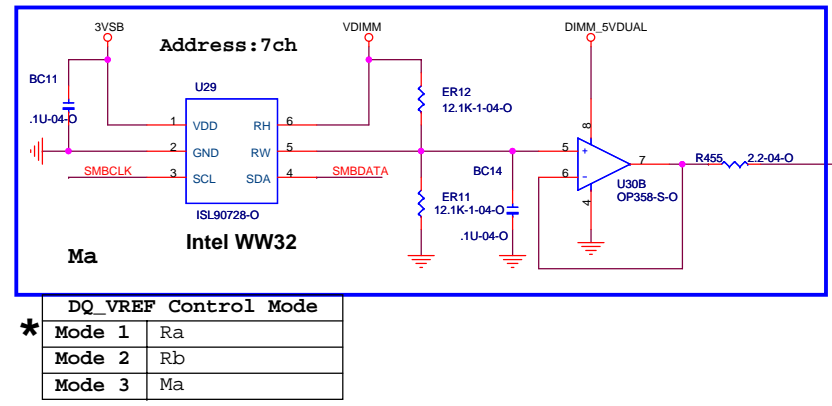
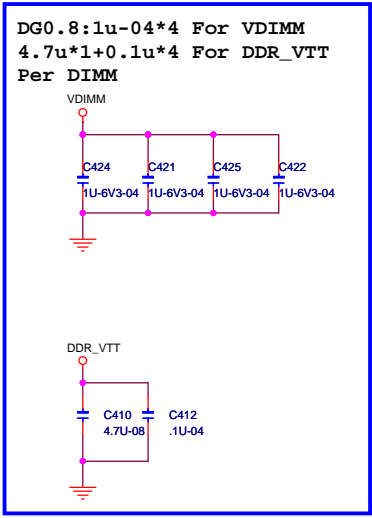
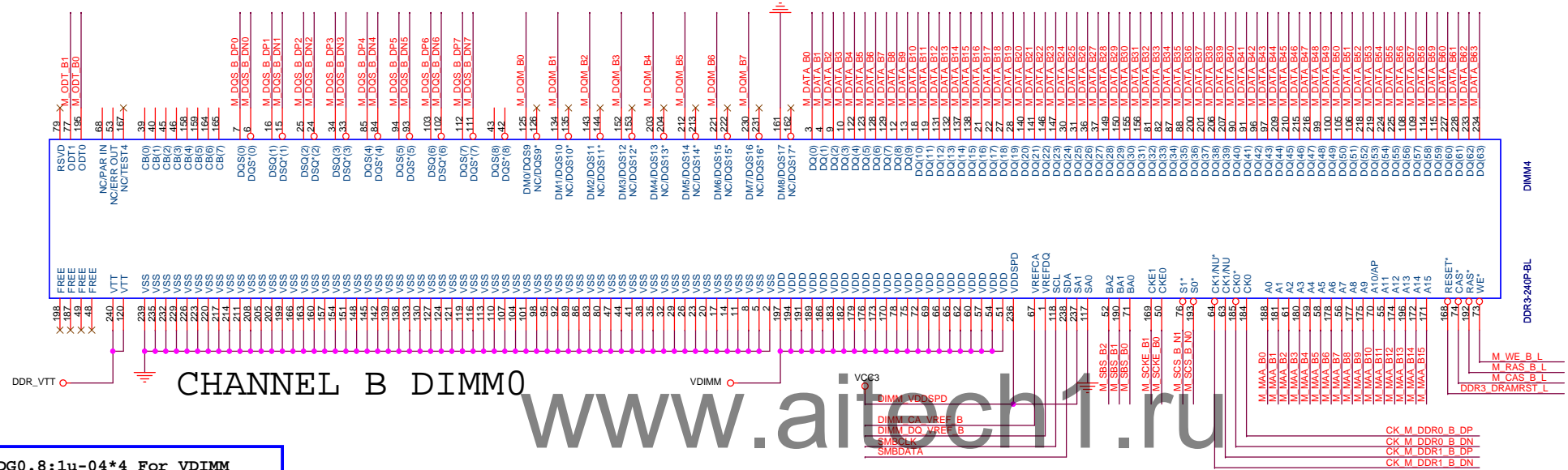
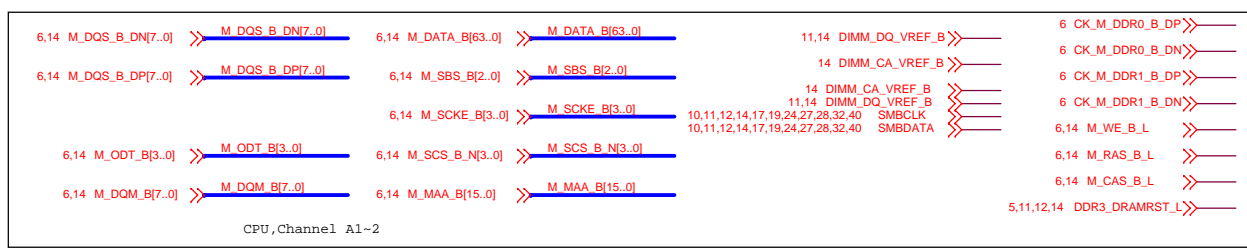
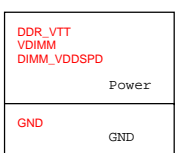
43

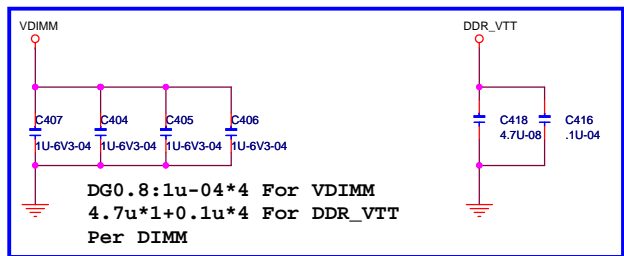
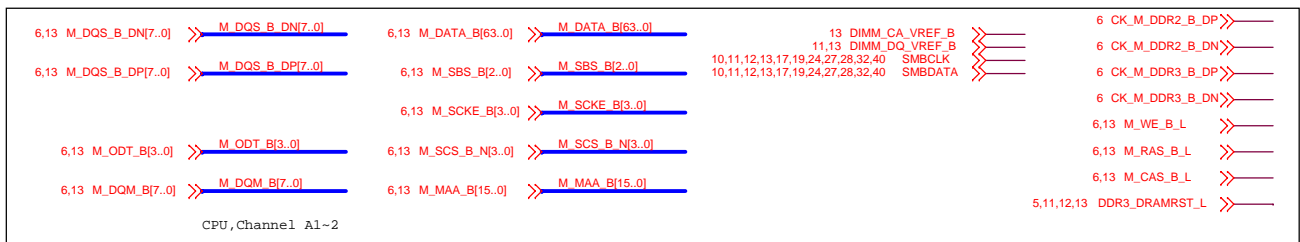


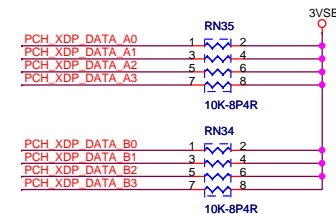
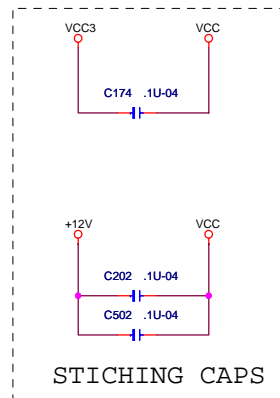
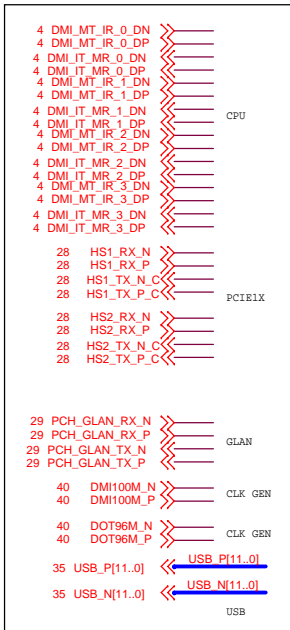


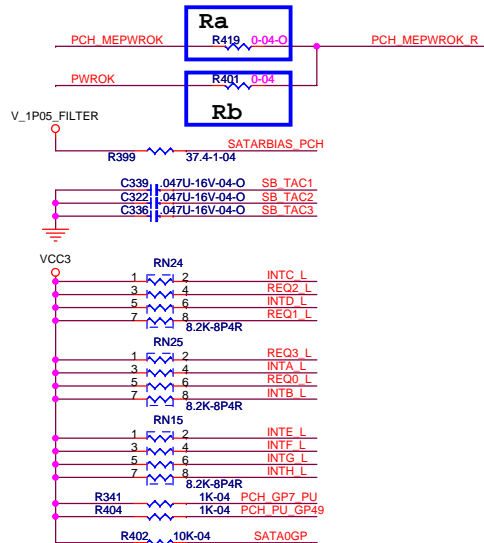
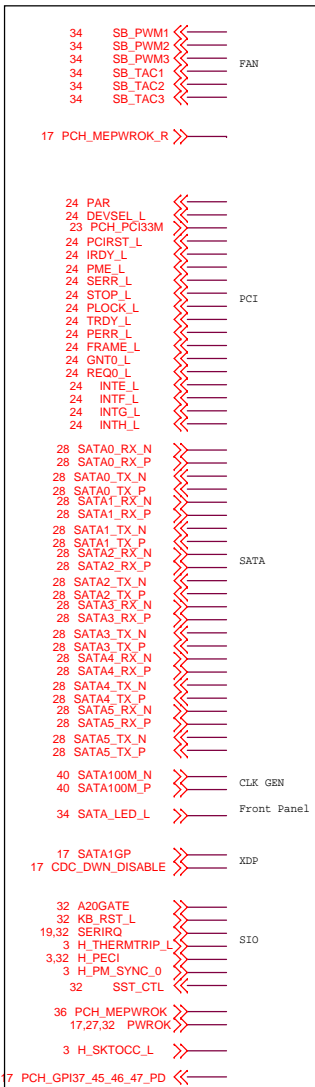
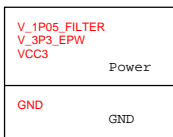




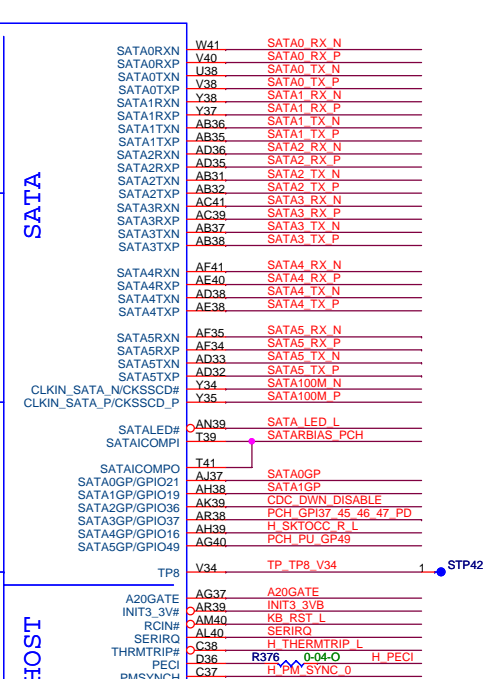
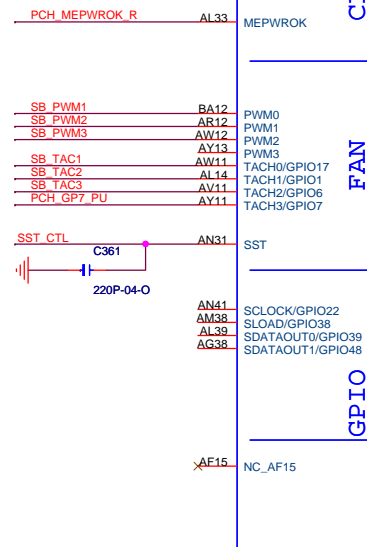




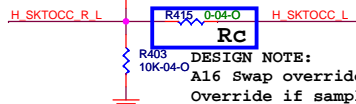




ME_PWROK	
AMT	Ra
Non-AMT	Rb



Stuff Rc for ME on CPU present detection

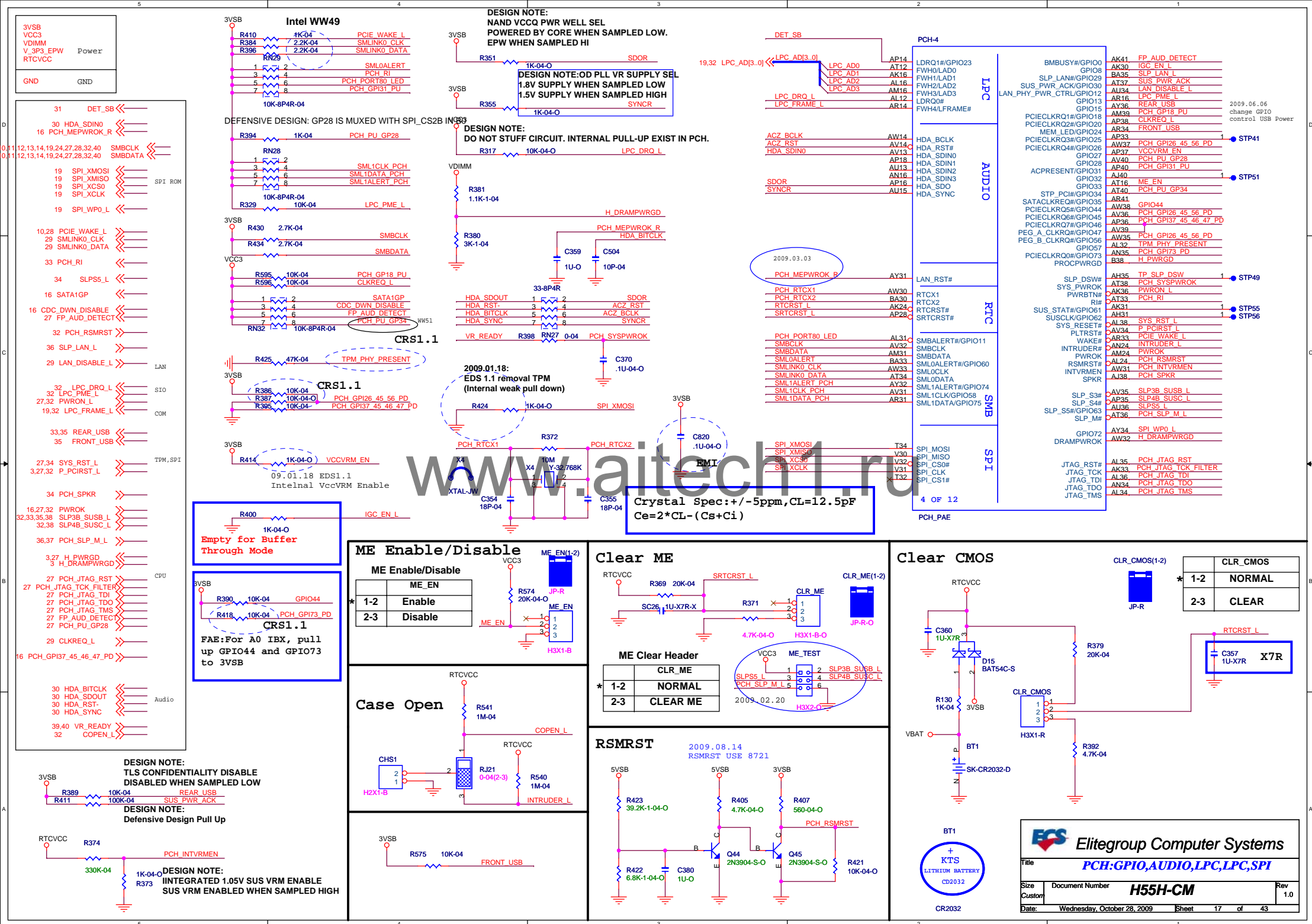


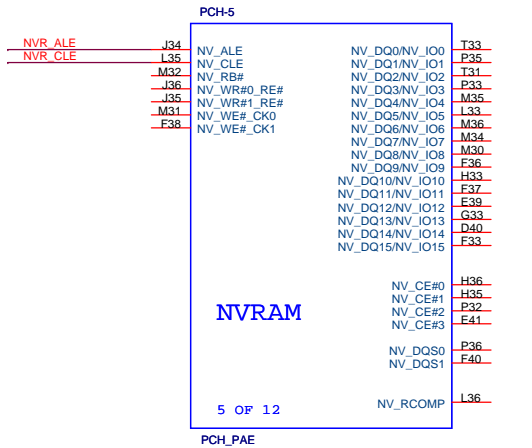
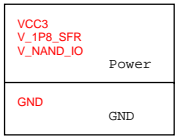
DESIGN NOTE:
A16 Swap override
Override if sampled low

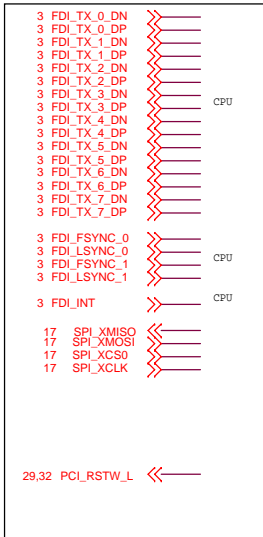
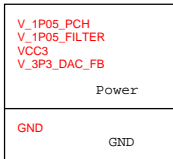
DESIGN NOTE:
DMI AC COUPLING
FULL VOLTAGE MODE WHEN SAMPLED LOW
Desktop Platform do't pull low

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

www.aitech1.ru

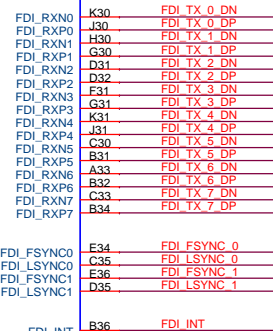




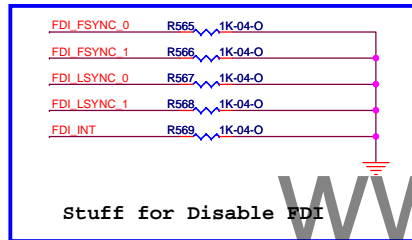


PCH-7

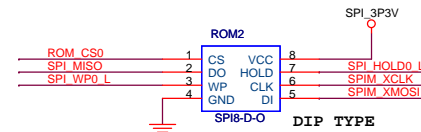
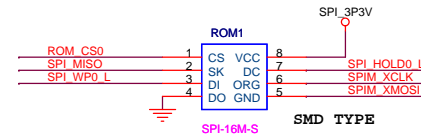
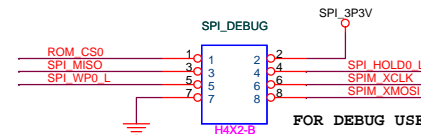
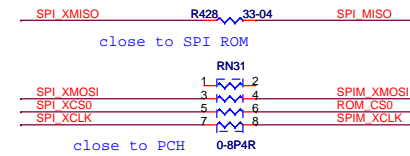
FDILINK



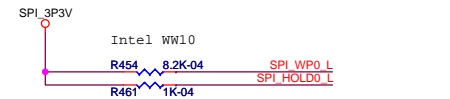
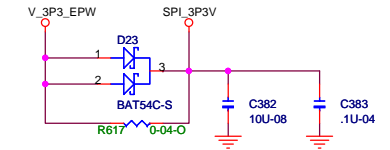
PCH_PAE



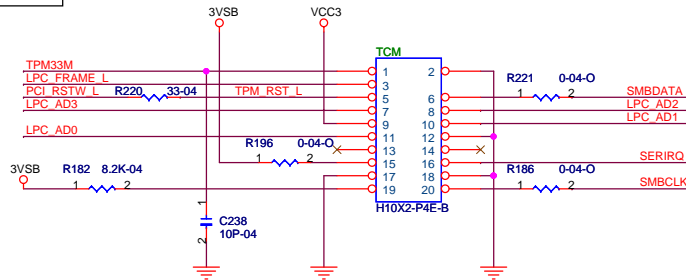
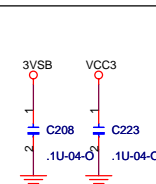
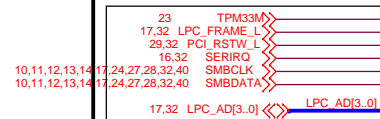
PCH FDI Link

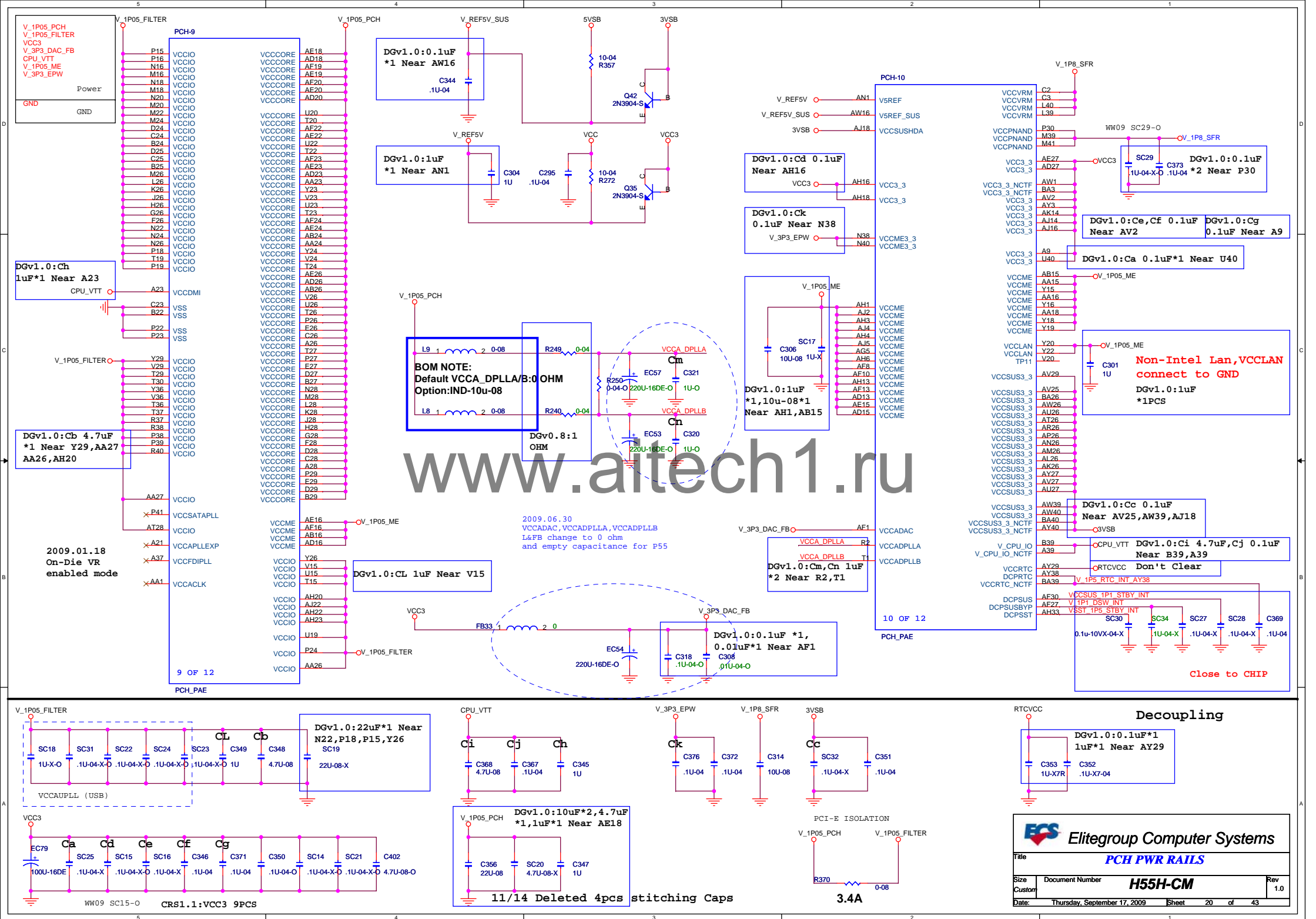


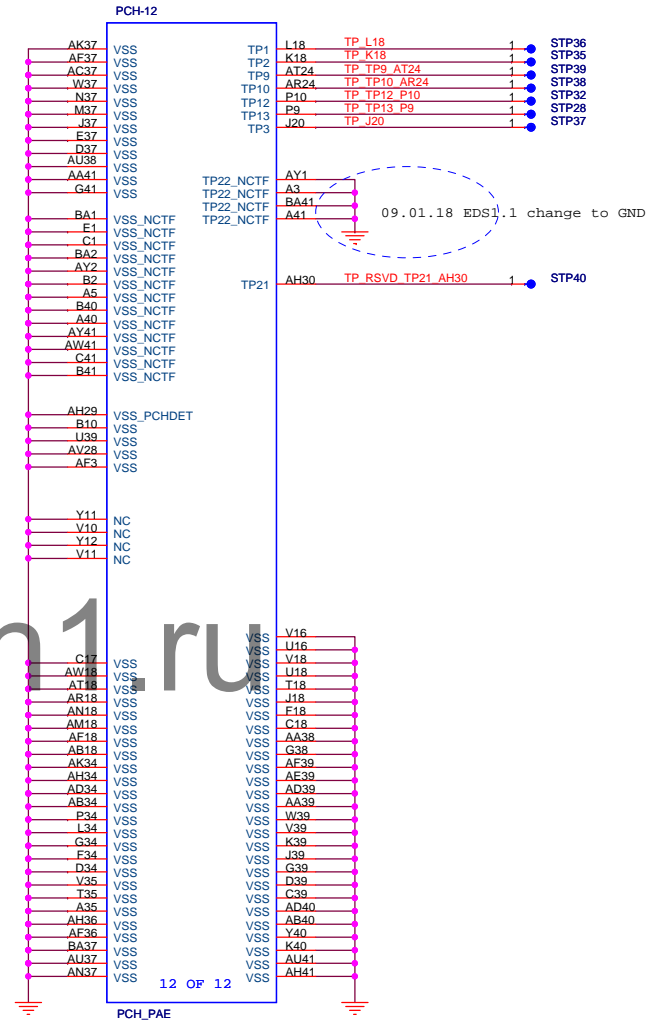
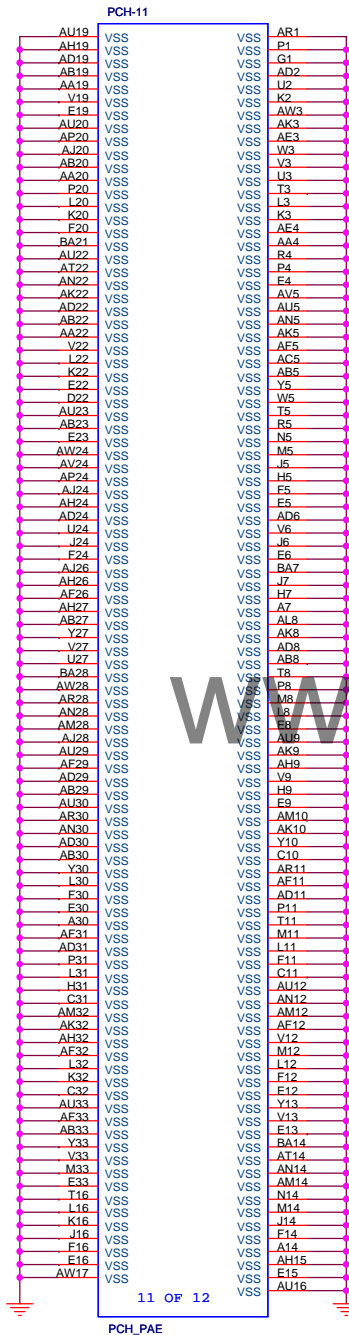
SPI ROM

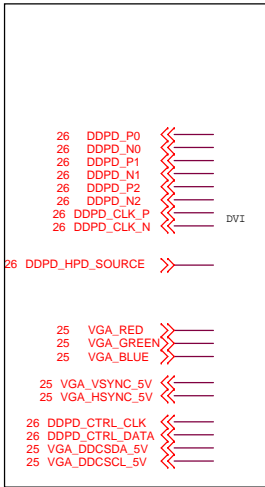
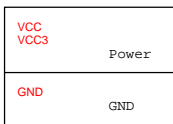


	BIOS_WP
Short	Protect
Open	Unprotect

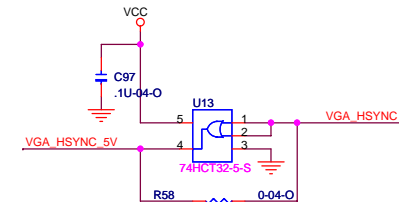
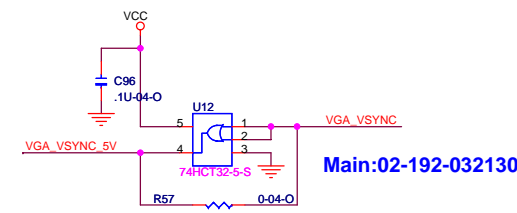
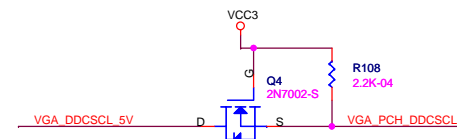
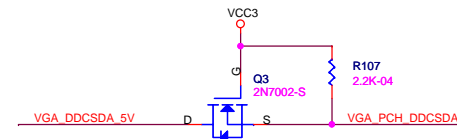
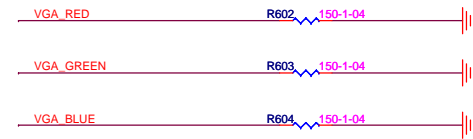
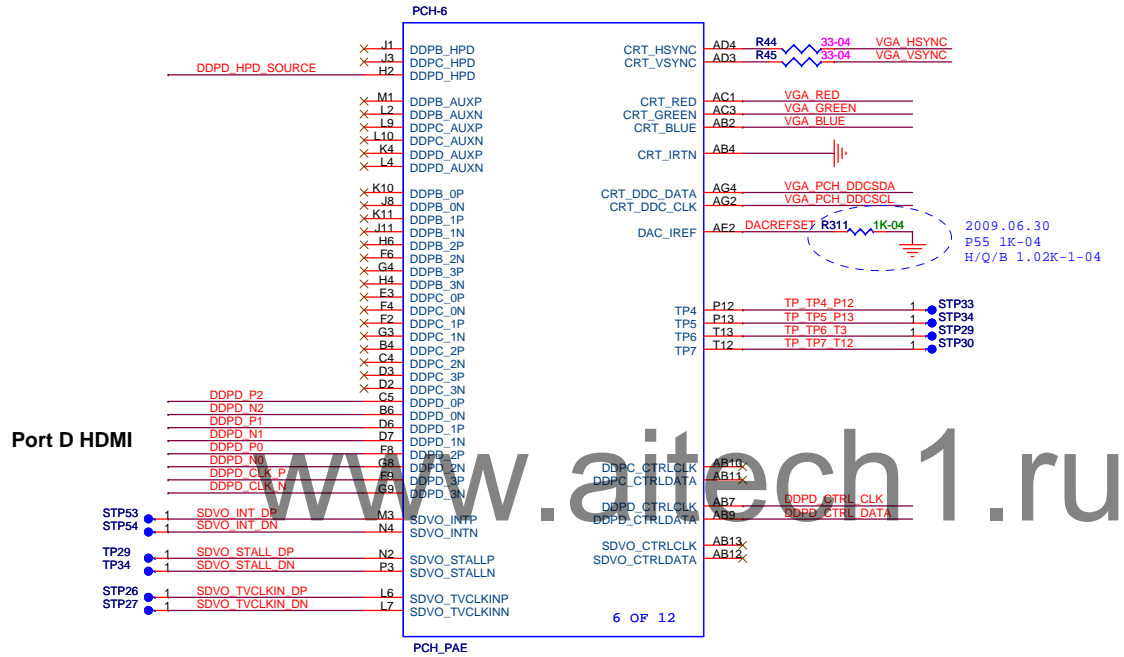




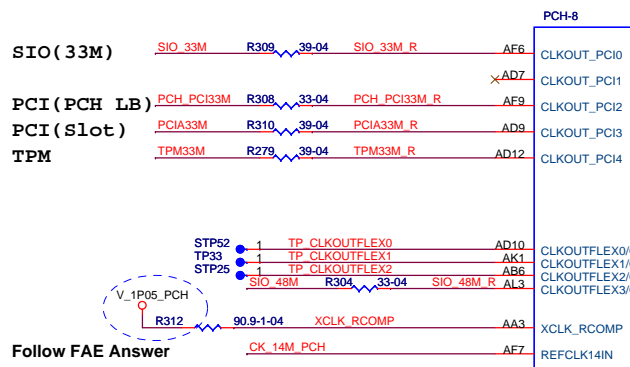
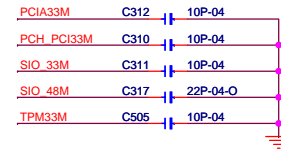
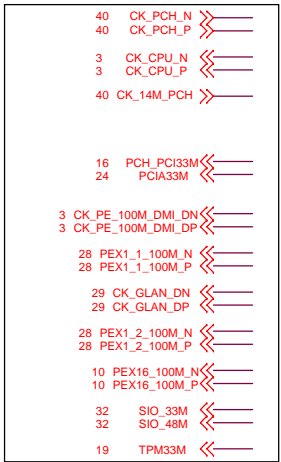
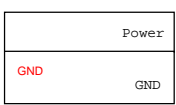




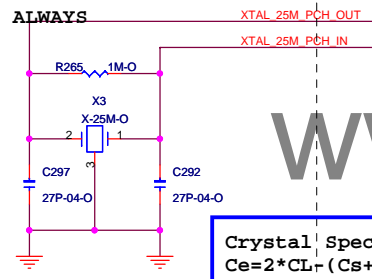
Port B: Capable of SDVO/HDMI/DVI/DP
Port C: Capable of HDMI/DVI/DP
Port D: Capable of HDMI/DVI/DP



Port	Strap	How to enable the port	How to Disable the Port
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC



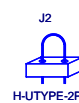
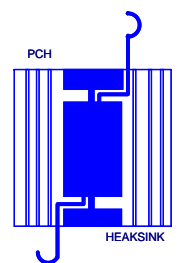
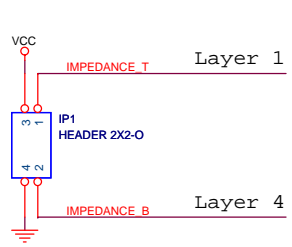
DESIGN NOTE:
STUFF ALWAYS



Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL (Cs+Ci)

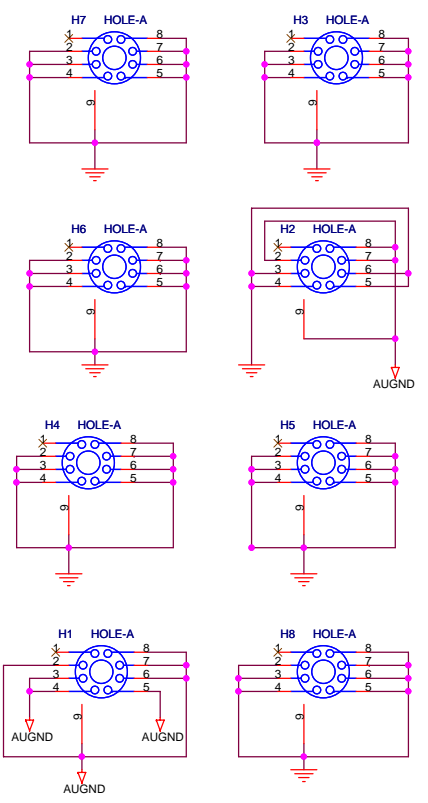
DESIGN NOTE:
R128 DAMPING RESISTOR
DO NOT CHANGE TO 0402

www.aitech1.ru



Main Part:20-120-013522
Substitute:20-120-013523

1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W



From CLK GEN

CPU(133M)

CPU(DMI)

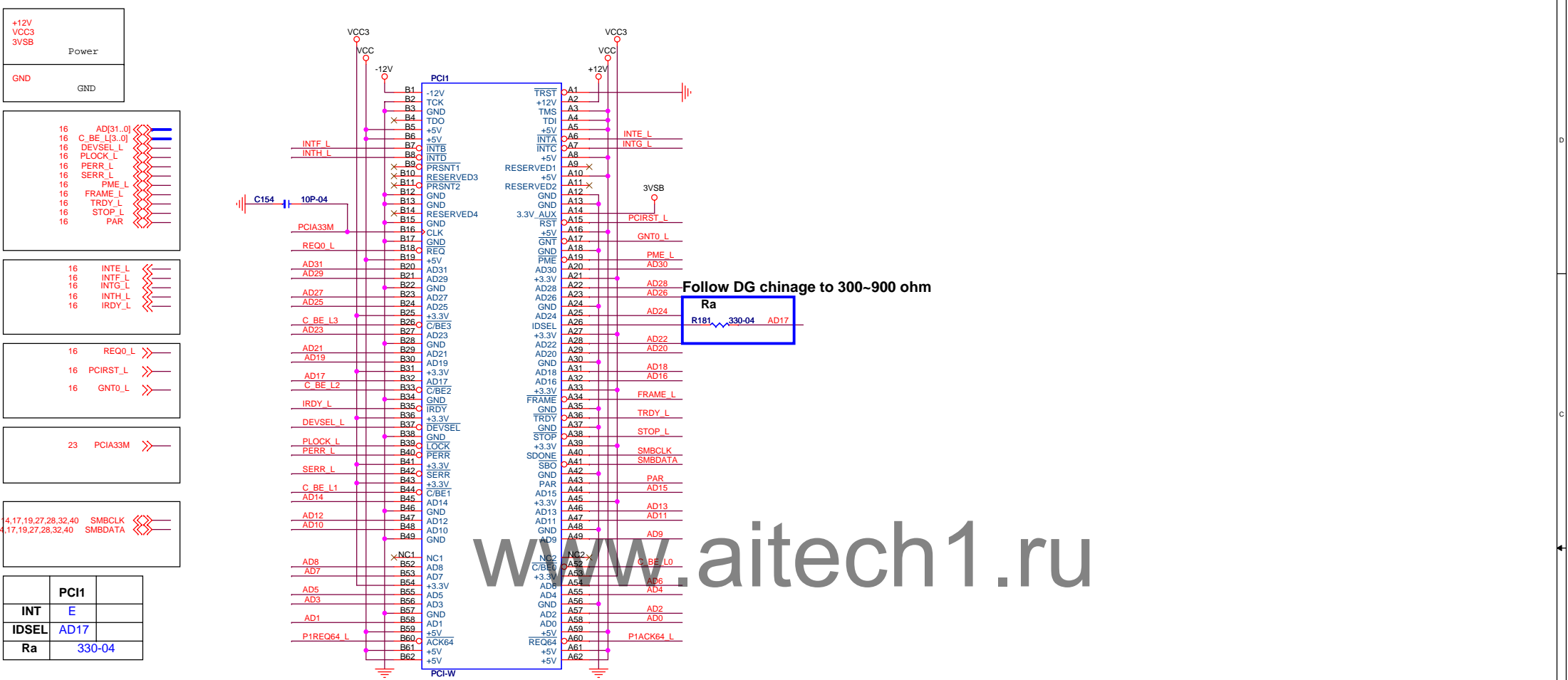
PCIE (X1)

Giga LAN

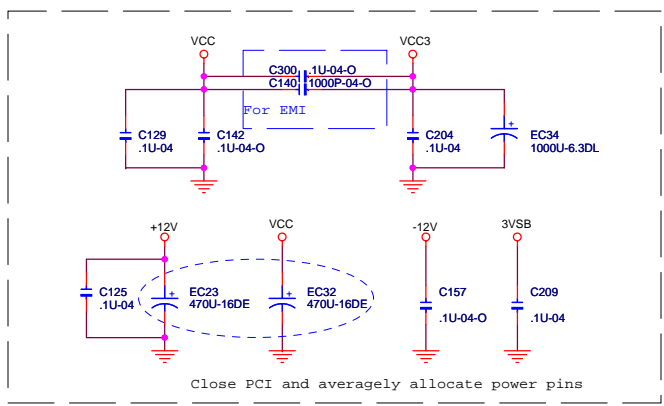
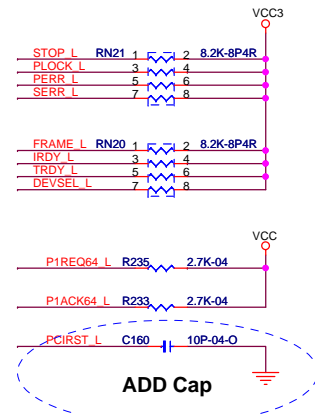
PCIE (1X2)

PCIE (16X)

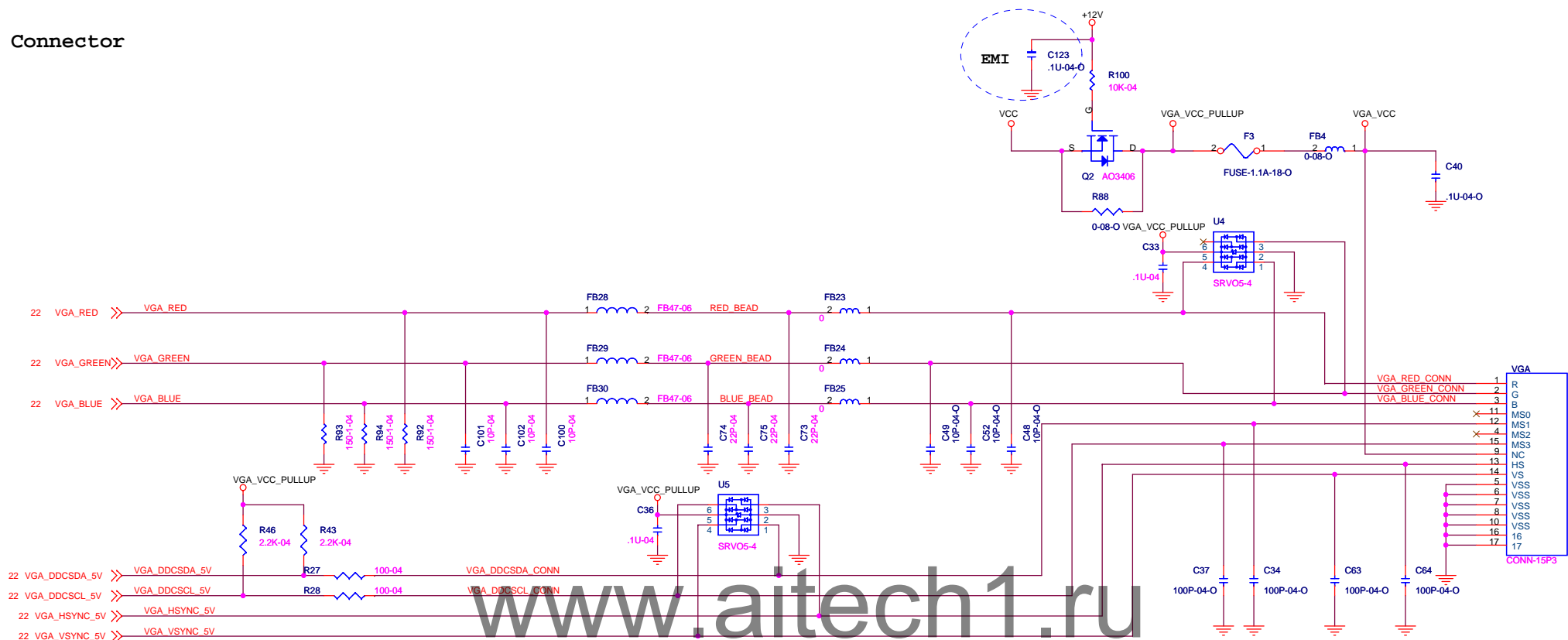
Elitegroup Computer Systems
PCH CLOCKS,STRAPS
Title
Size Custom Document Number **H55H-CM** Rev 1.0
Date: Thursday, September 17, 2009 Sheet 23 of 43

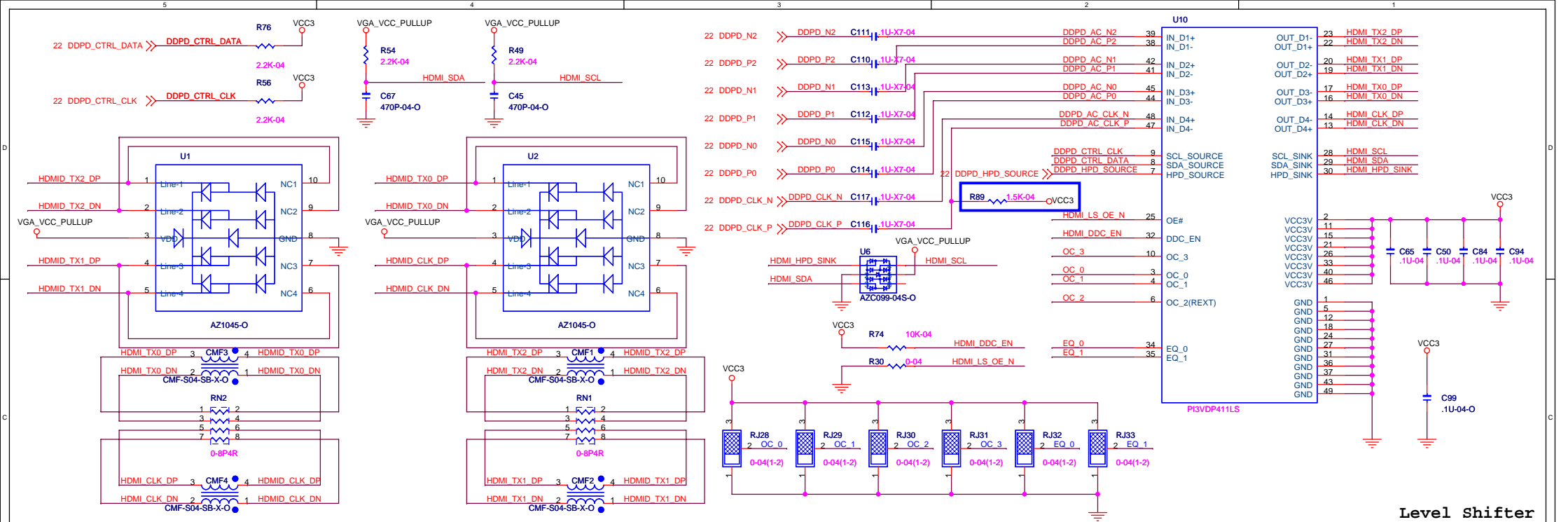


	PCI1	
INT	E	
IDSEL	AD17	
Ra	330-04	



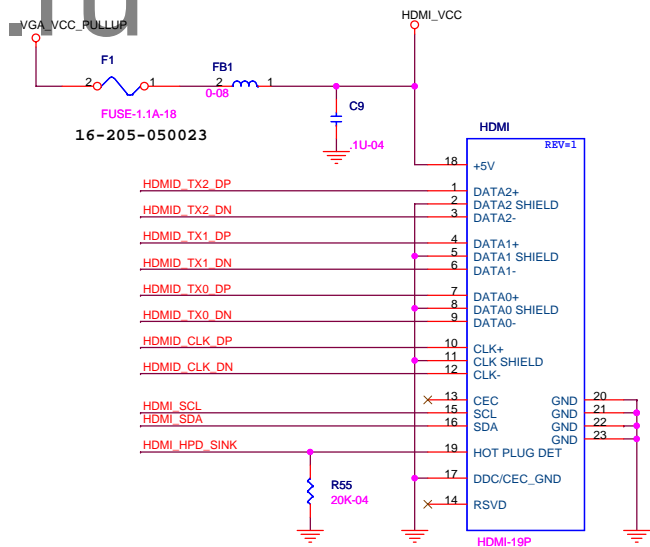
VGA Connector

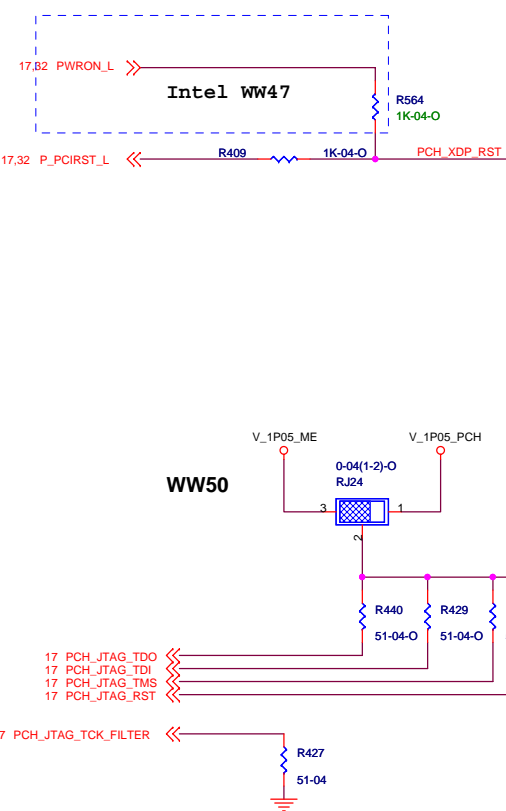
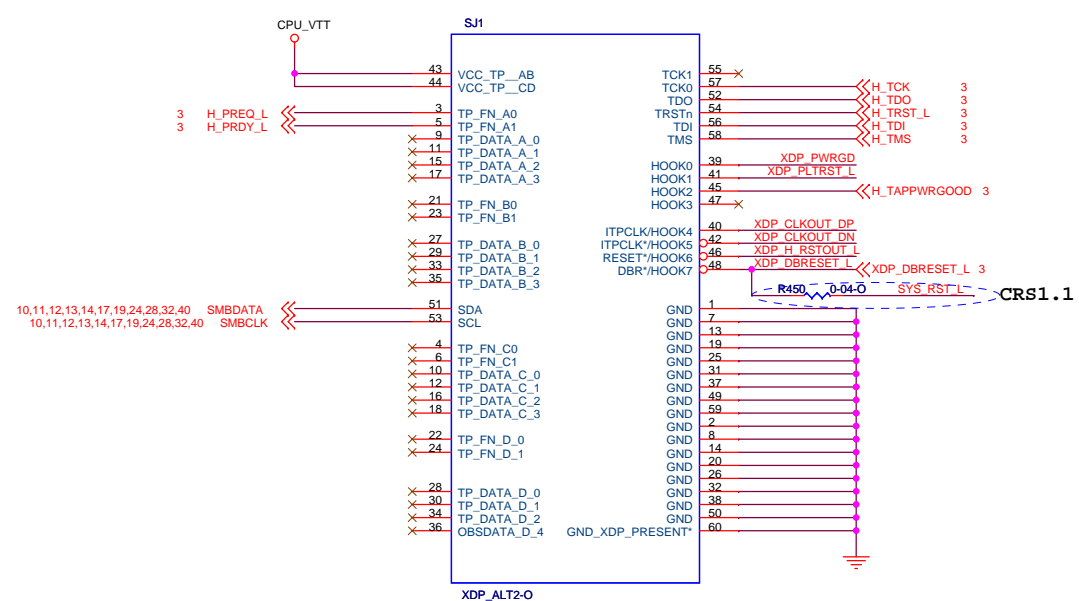
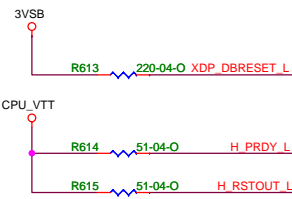
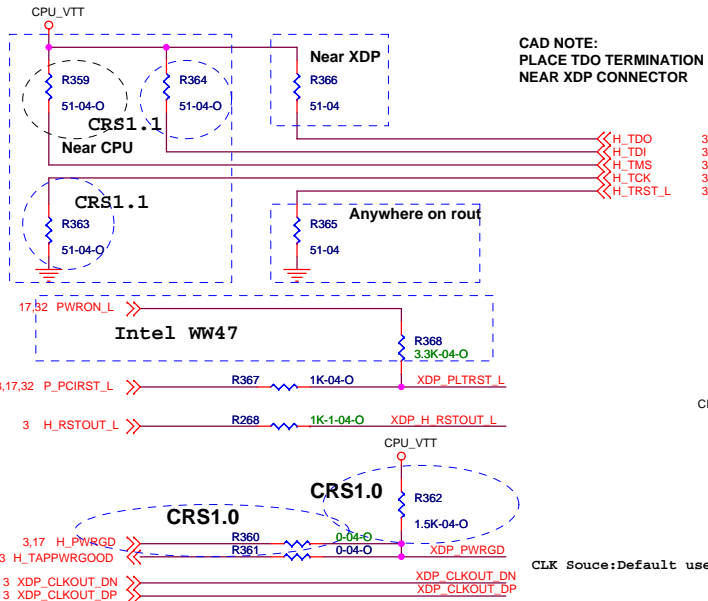




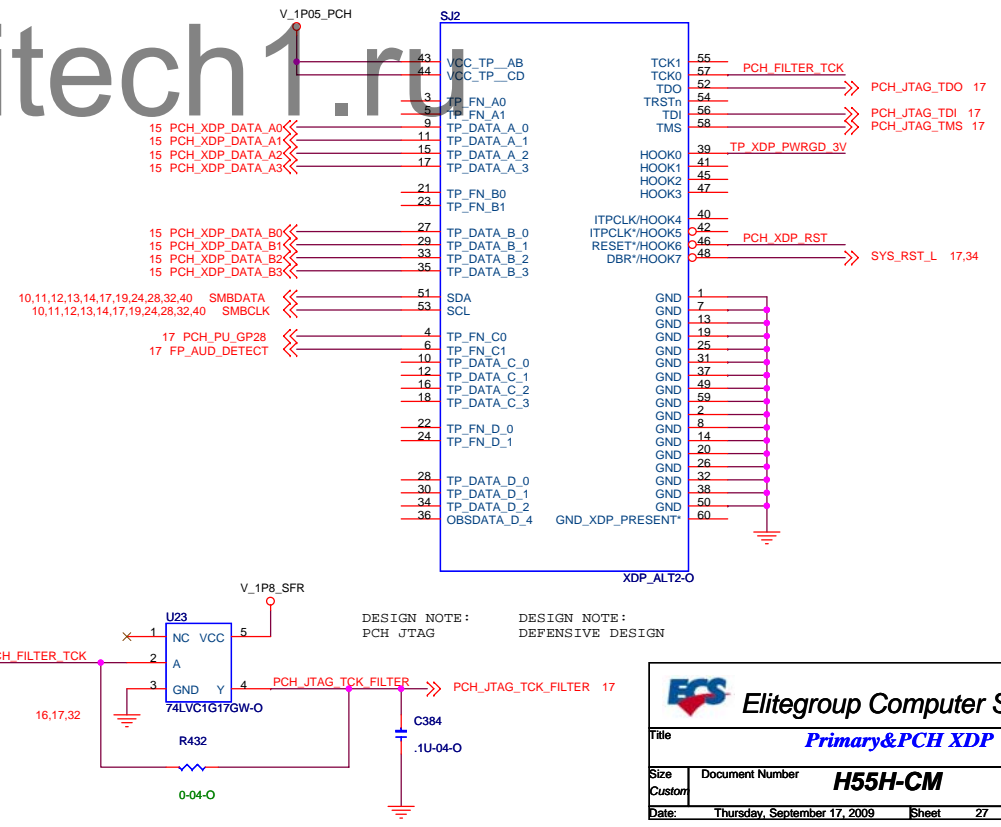
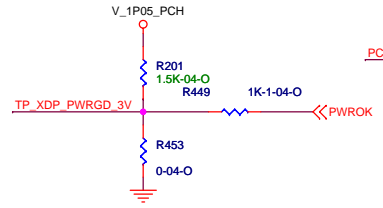
Level Shifter

HDMI Connector





PCH PIN	RefDes	ES1	ES2	Production Systems
TDO	R440	No Stuff	100 Ohms	51 Ohms
TMS	R433	100 Ohms	100 Ohms	51 Ohms
TDI	R429	100 Ohms	100 Ohms	51 Ohms
TRST#	R420	10K Ohms	10K Ohms	51 Ohms
	RJ24	0(2-3)	0(2-3)	0(1-2)



DESIGN NOTE:
DEFAULT EMPTY SITE ON PAGE 94: XDP_PWRGD RES (R108PR) TO VTT_OUT_RIGHT
DEFAULT EMPTY SITE ON PAGE 123: XDP_PWRGD RES (R3S3EV) TO V_FSB_VTT
DEFAULT STUFF SITE: (R662EV) TO TP_XDP_PWRGD

DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN

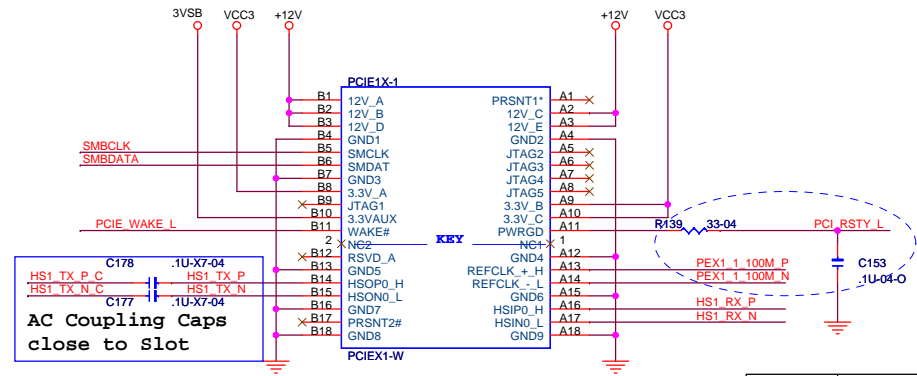
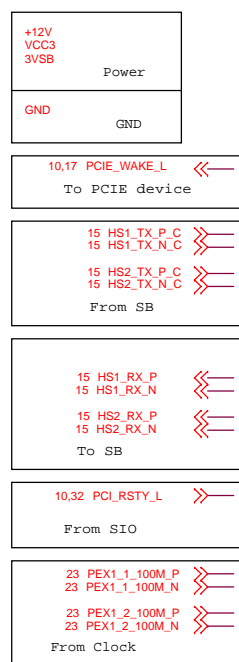
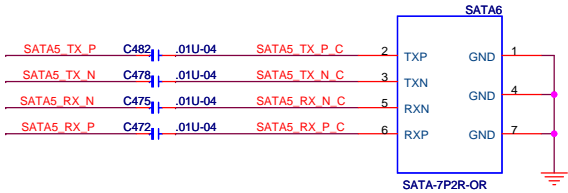
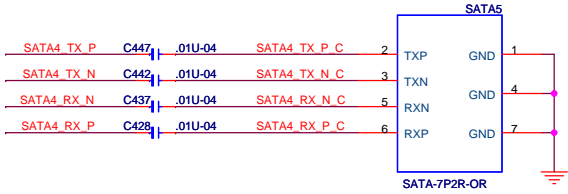
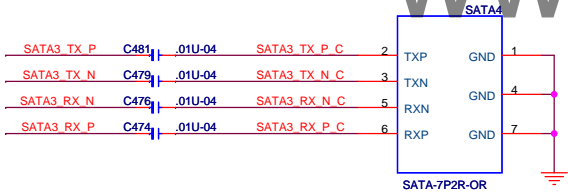
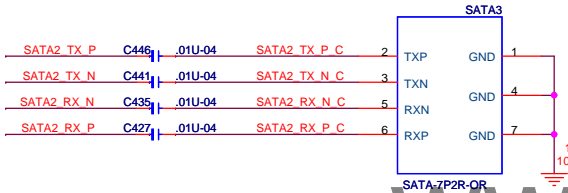
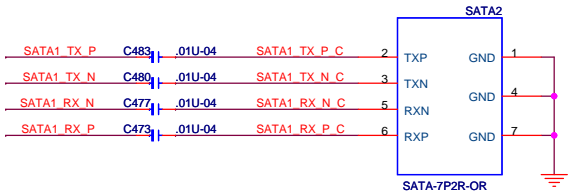
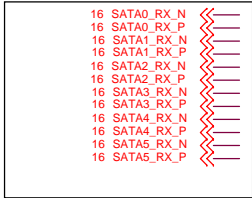
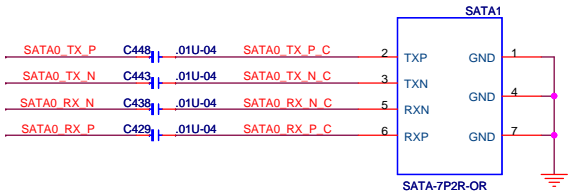
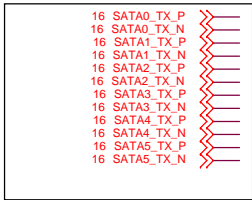
Elitegroup Computer Systems

Primary&PCH XDP

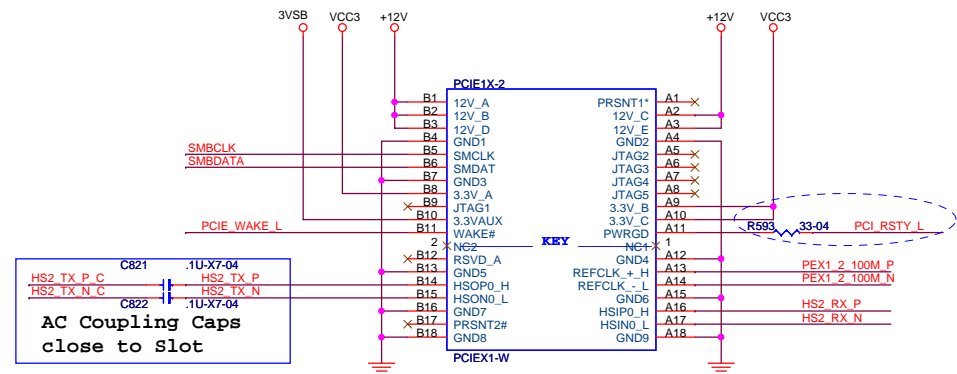
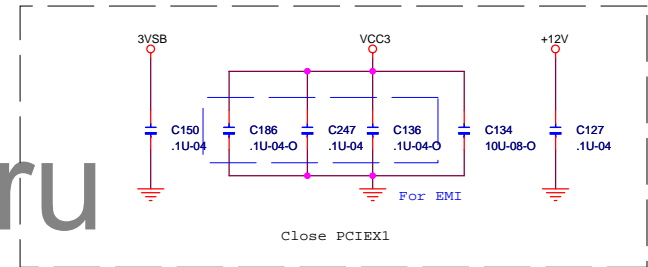
File

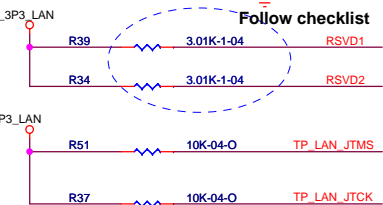
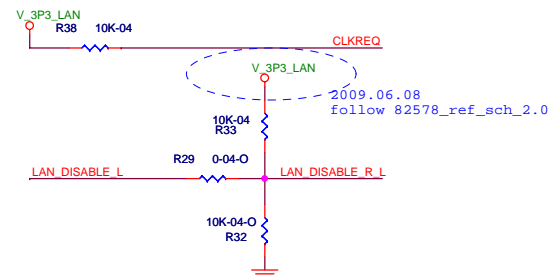
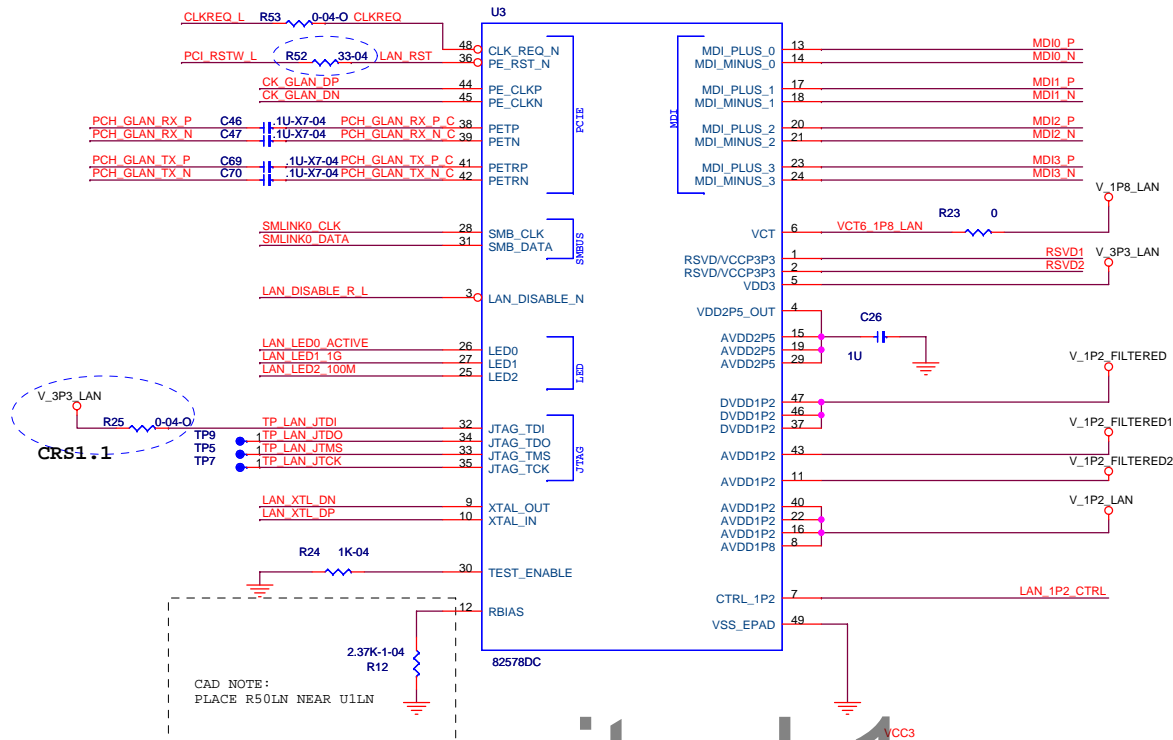
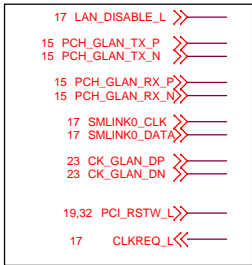
Size Document Number **H55H-CM** Rev 1.0

Date: Thursday, September 17, 2009 Sheet 27 of 43

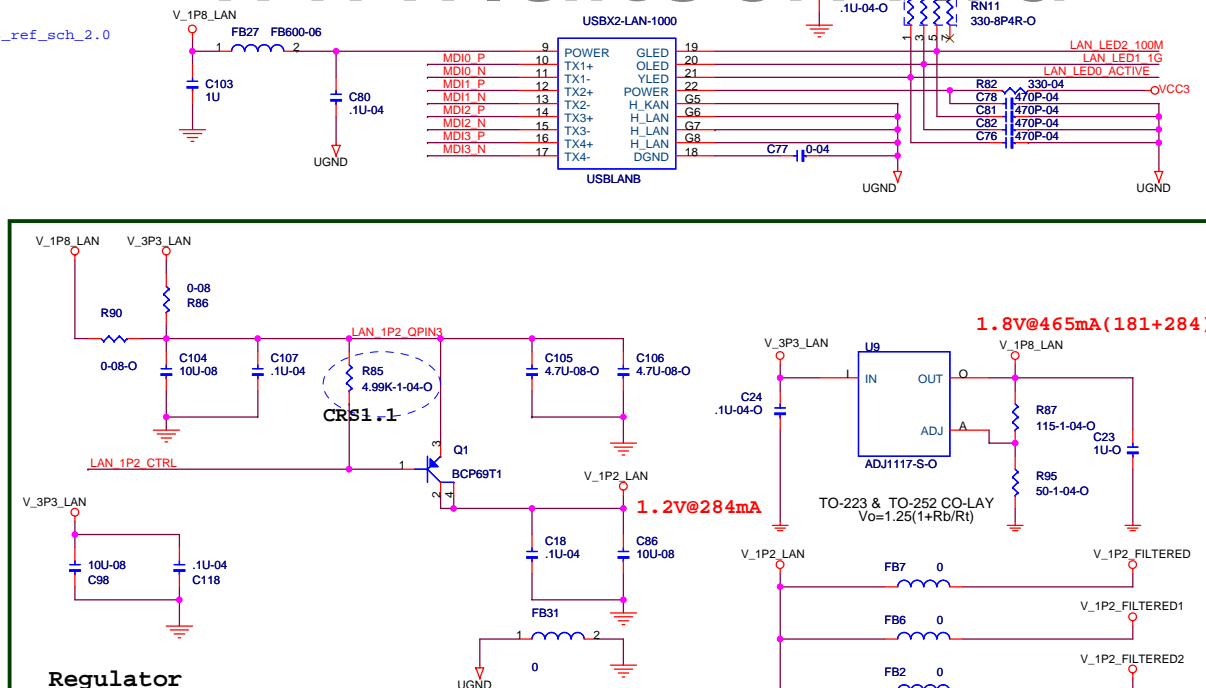
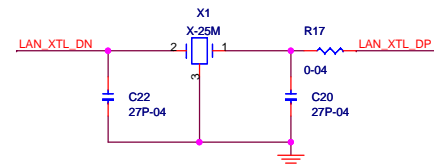


	PC_RST
INTEL	SIO:PCI REST
AMD	NB:PCIE REST
NV?	



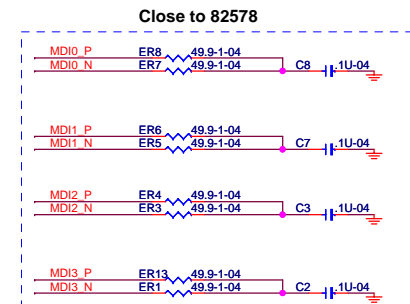
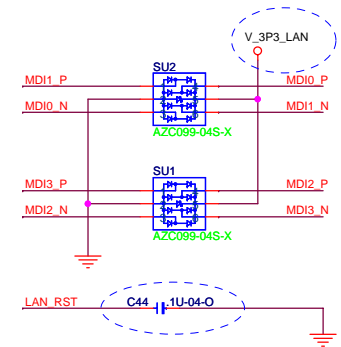


Crystal Spec: $\pm 30\text{ppm}$, $CL=20\text{pF}$
 $Ce=2*CL-(Cs+Ci)$

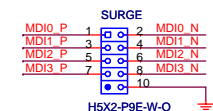


WOL	Status	Yellow	Gre/Ora
Don't Care	No link	OFF	OFF
OFF	S3/S4/S5	OFF	OFF
ON	10M,Inactive	OFF	OFF
ON	10M,Active	YB	OFF
ON	100M/Inactive	OFF	G
ON	100M/Active	YB	G
ON	1G,Inactive	OFF	O
ON	1G/Active	YB	O

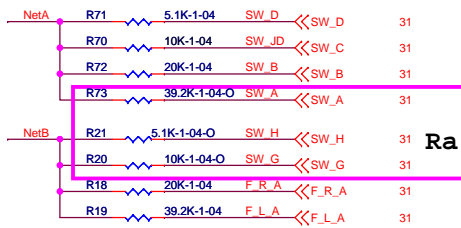
Remark: Y/G/O-->Color, B-->Blinking



Surge for TongFang

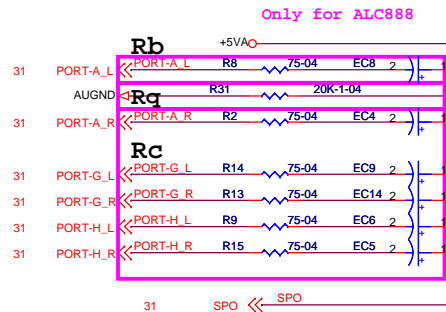


Resistors Networks

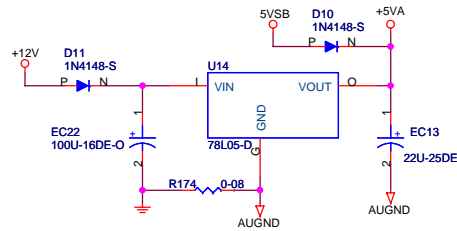


Only for ALC888

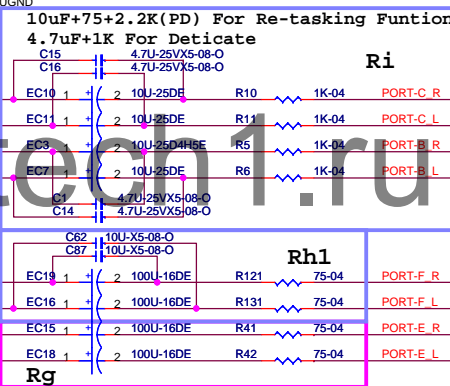
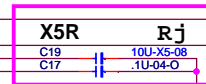
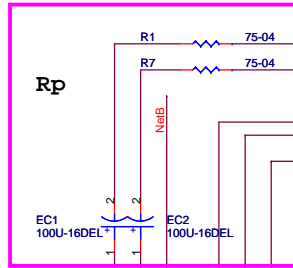
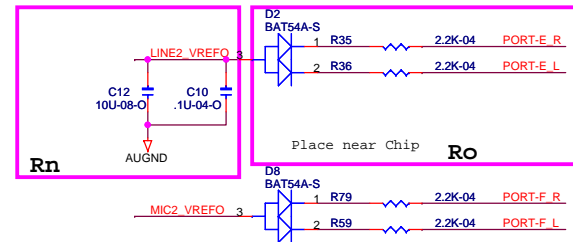
Place near Chip



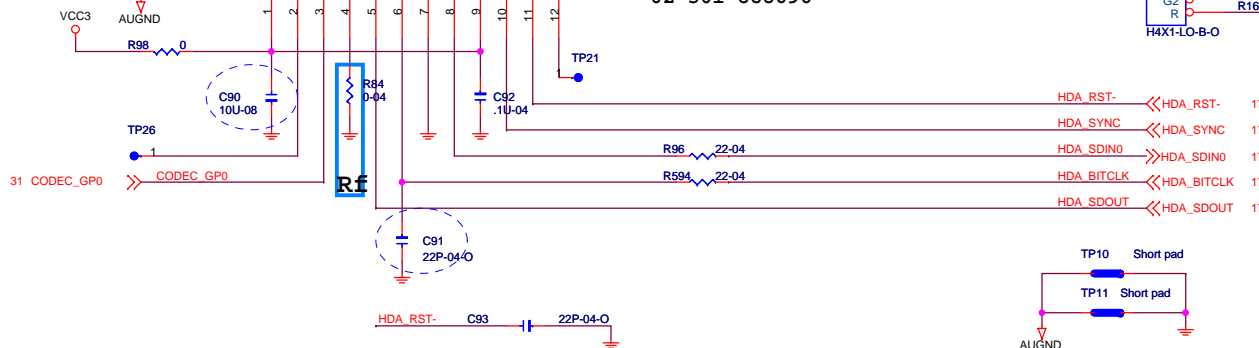
Only for ALC888

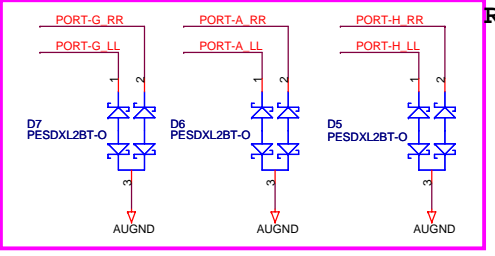
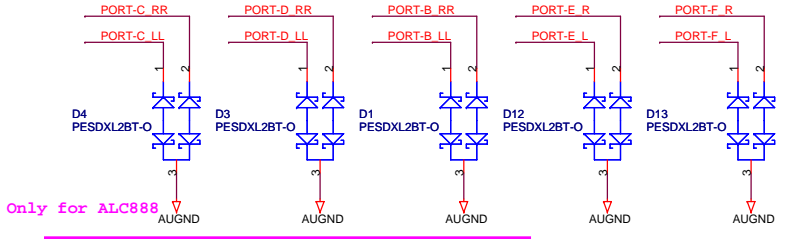
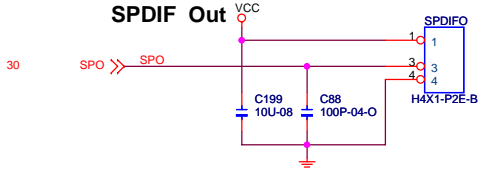
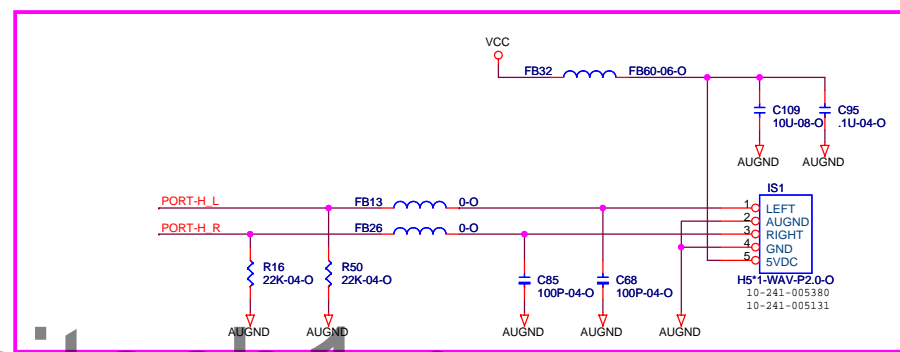
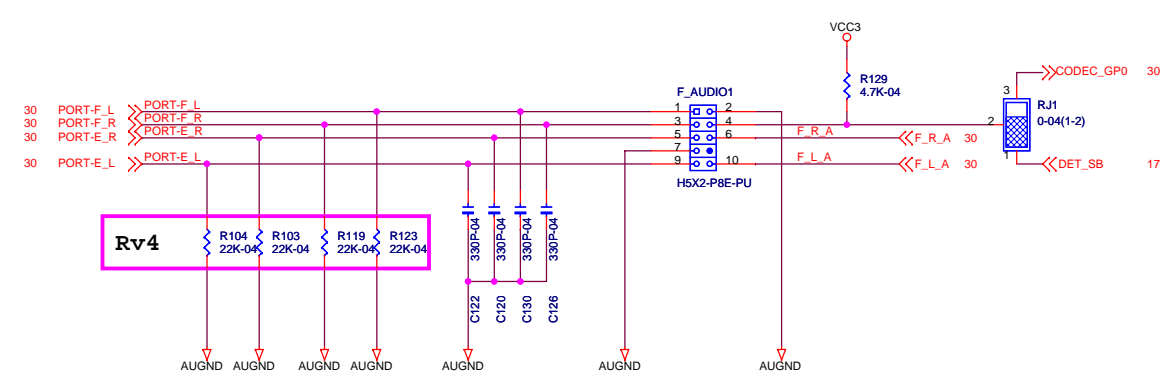
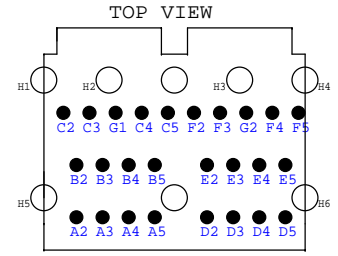
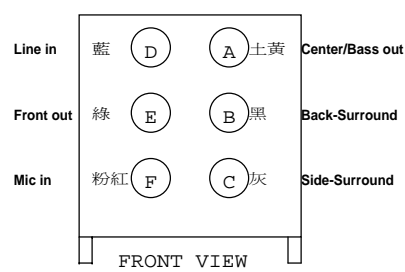
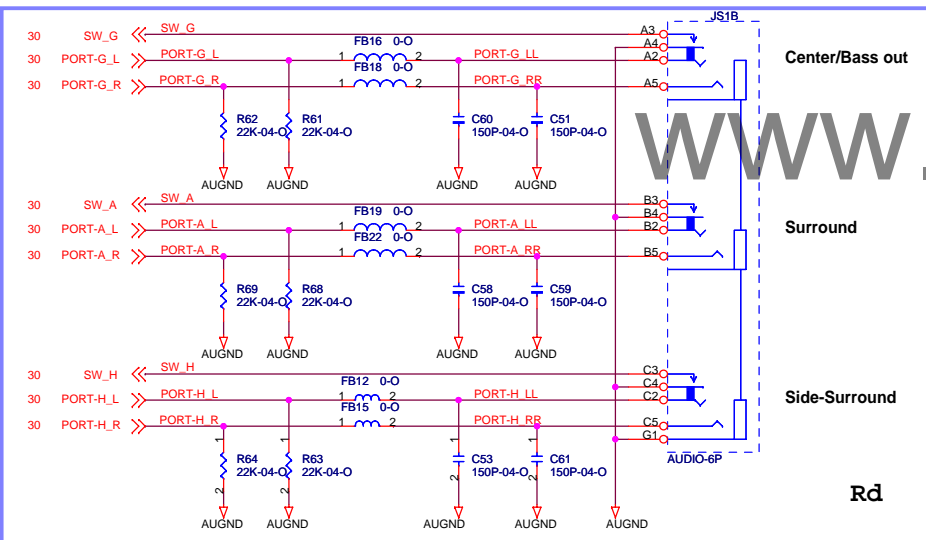
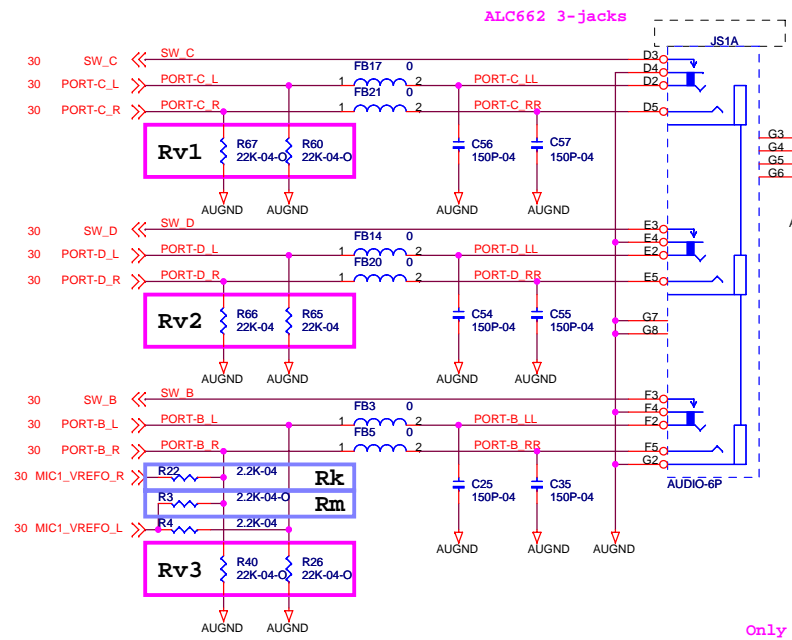


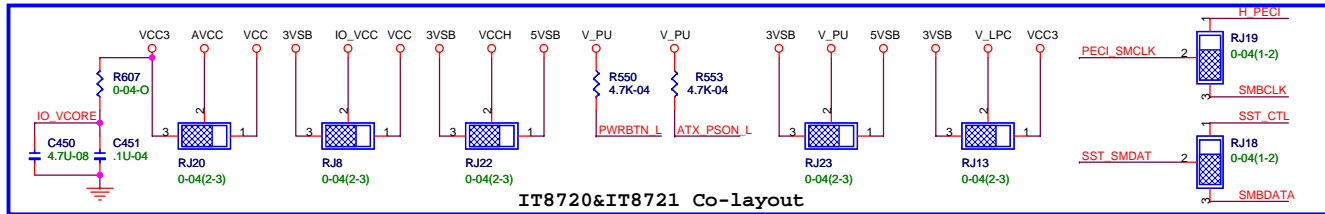
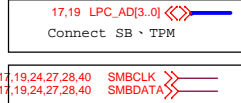
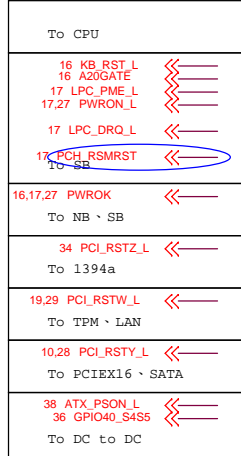
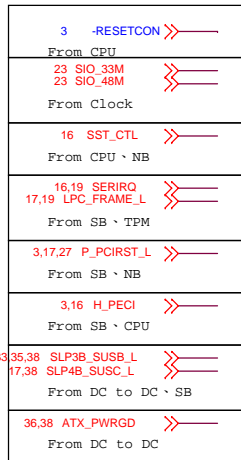
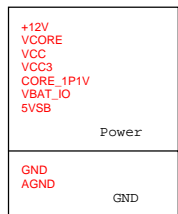
Verfourt bias for stereo microphone.



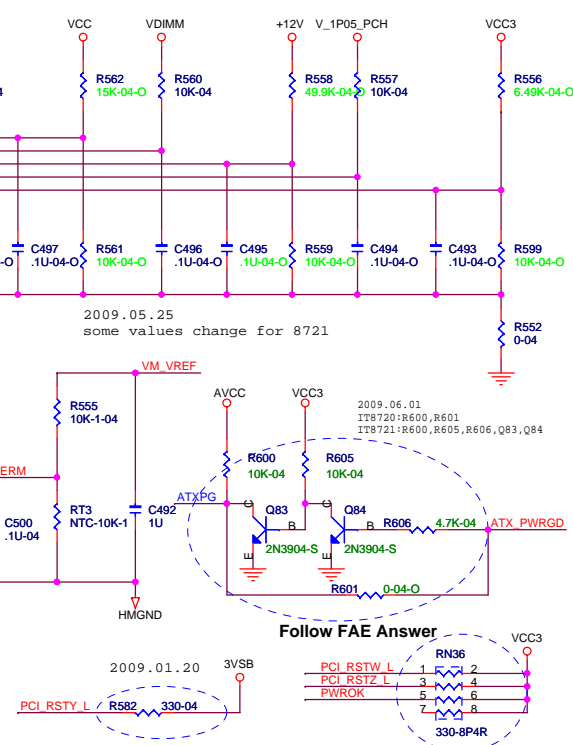
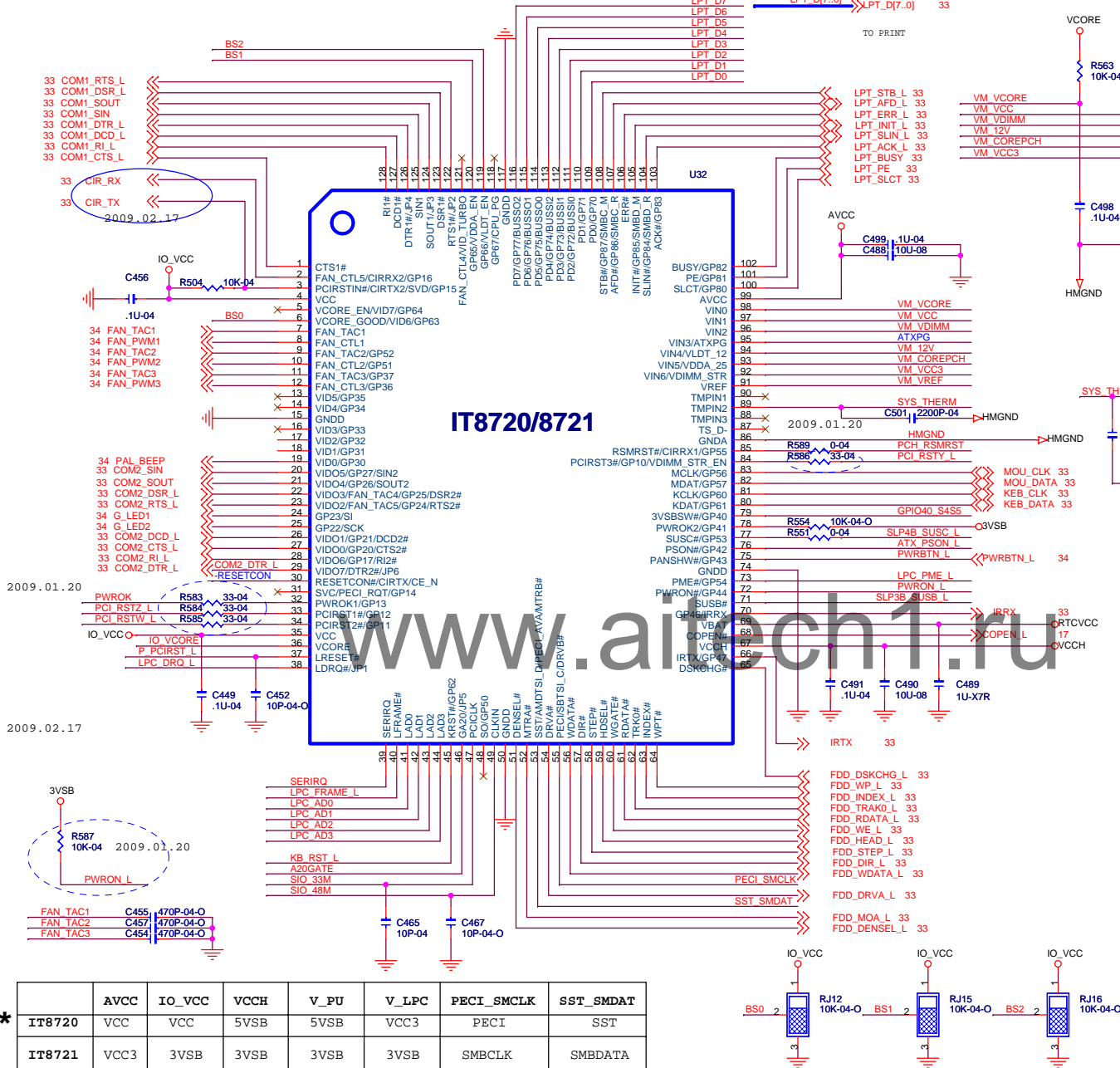
	ALC888-VC	ALC662-VC	VT1708B
Ra	Stuff	Open	Open
Rb	0 OHM	0 OHM	0 OHM
Rc	100u+75	100u+75	220u+0
Rd	100u+75	100u+75	10u+0
Re	10u+75	10u+75	10u+0
Rf	10u	10u	10u+0.1u
Rg	2.2K	2.2K	Open
Rh1	Open	Open	2.2K
Ri	Open	Open	Stuff
Rj	Open	Open	Open
Rk	Open	Open	Open
Rl	Open	Open	Open
Rm	Open	Open	Open
Rn	Open	Open	Open
Ro	Open	Open	Open
Rp	100u+75	100u+75	220u+0
Rq	20K	20K	5.1K
Rv1~4	2.2K	2.2K	Open







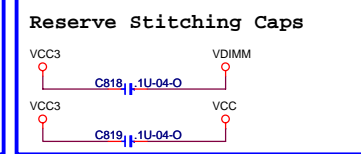
IT8720&IT8721 Co-layout

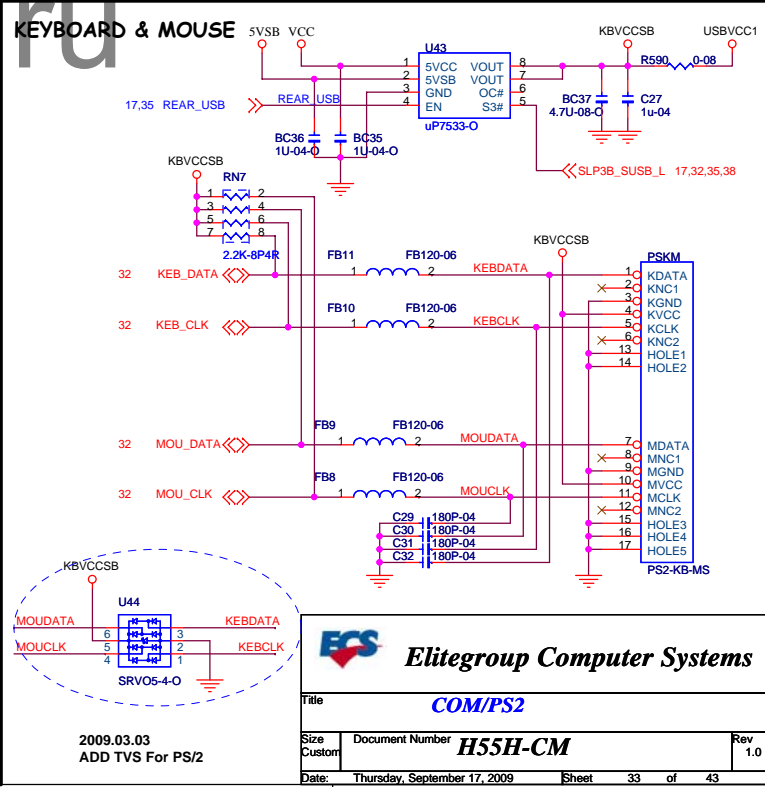
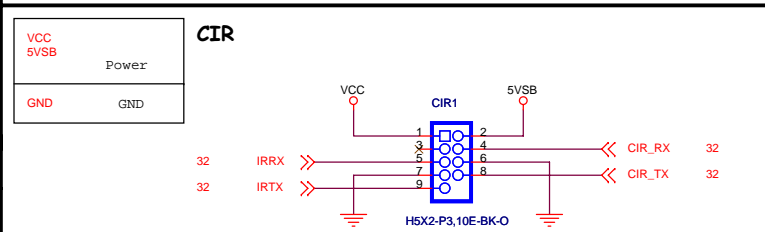
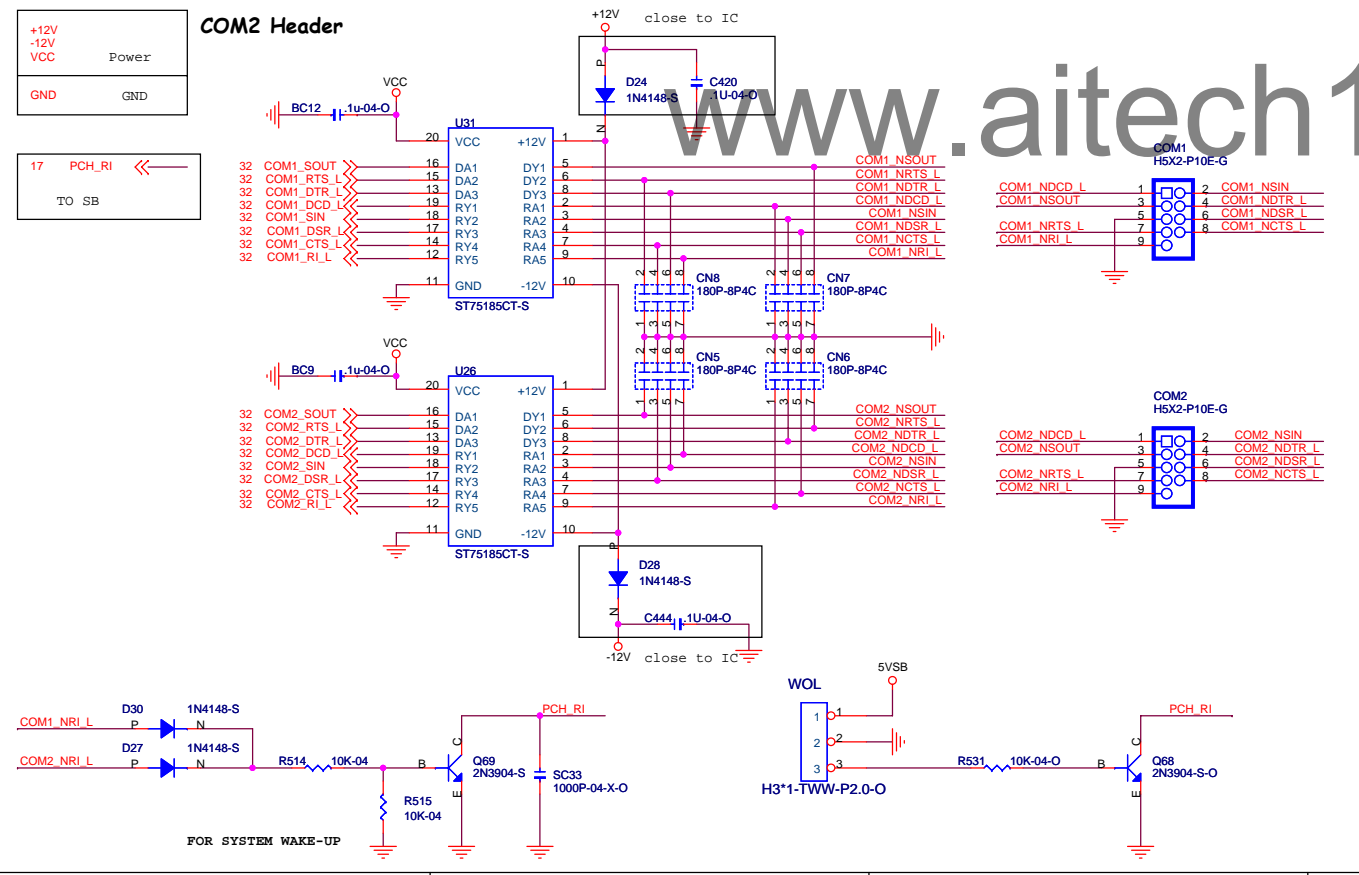
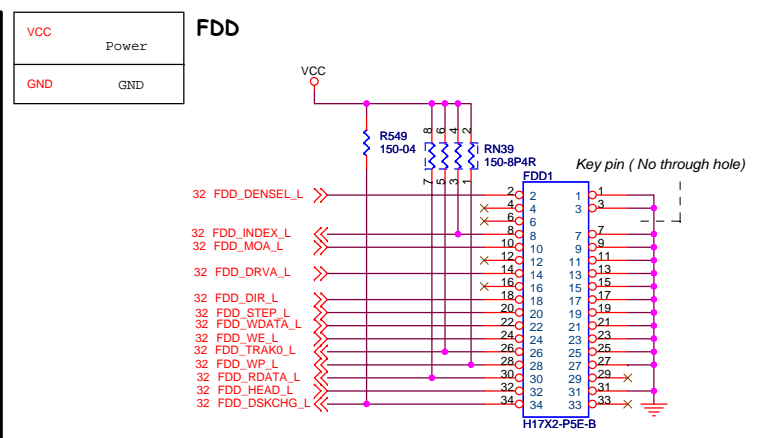
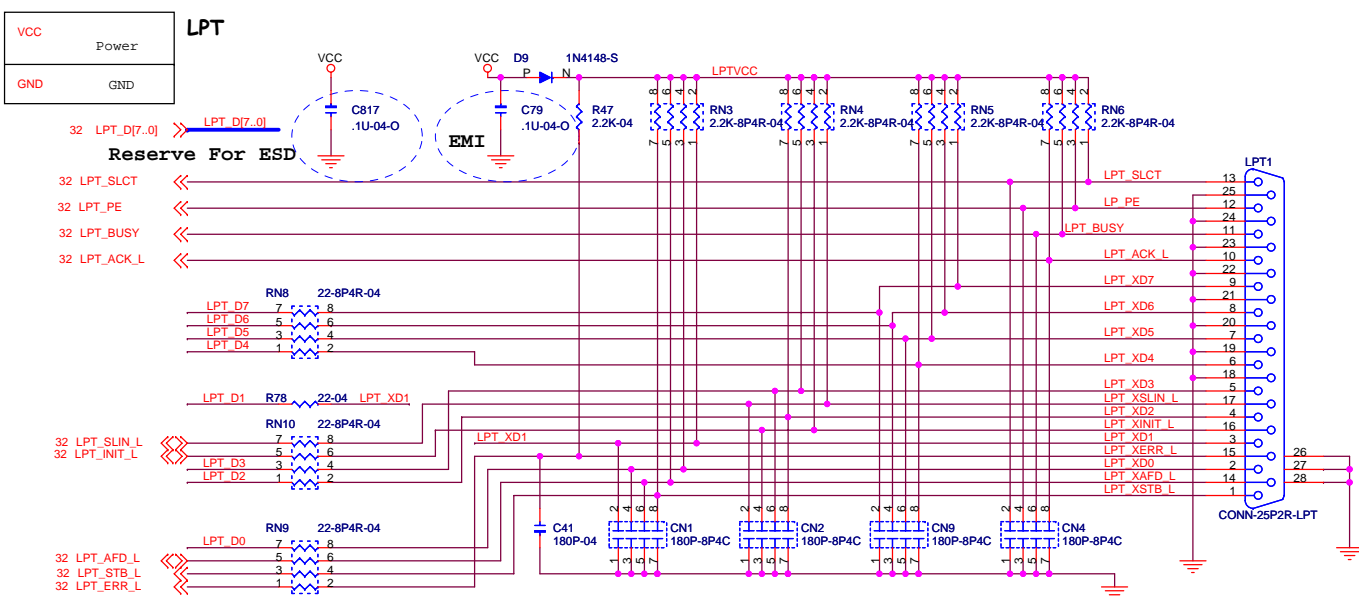


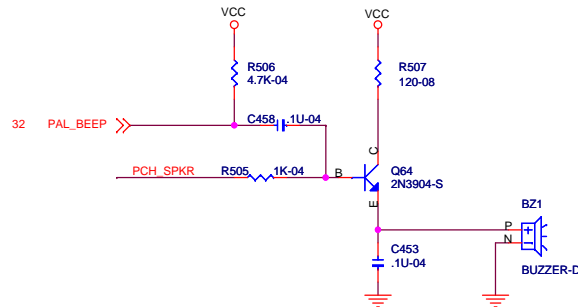
IT8721 Power On Strapping Options

Symbol	value	Description
JP2	11	Disable VID output pins
Pin 122	01	Intel Platform Enable VID output pins
JP6	10	AMD Platform Enable SVD/SVC Output
Pin29	00	AMD Platform Enable VIDO0-7
JP3	1	Disabled.
Pin 124	0	Flash I/F Address Segment 1 is enabled
JP4	1	K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
JP3	11	Default Index 15h/16h/17h is 40h 50%
Pin 124	10	Default Index 15h/16h/17h is 7Fh 0%
JP5	01	Default Index 15h/16h/17h is 00h 100%
Pin 46	00	Default Index 15h/16h/17h is 20h 75%
JP5	1	Disable WDT to rest PWROK
Pin46	0	Enable WDT to rest PWROK

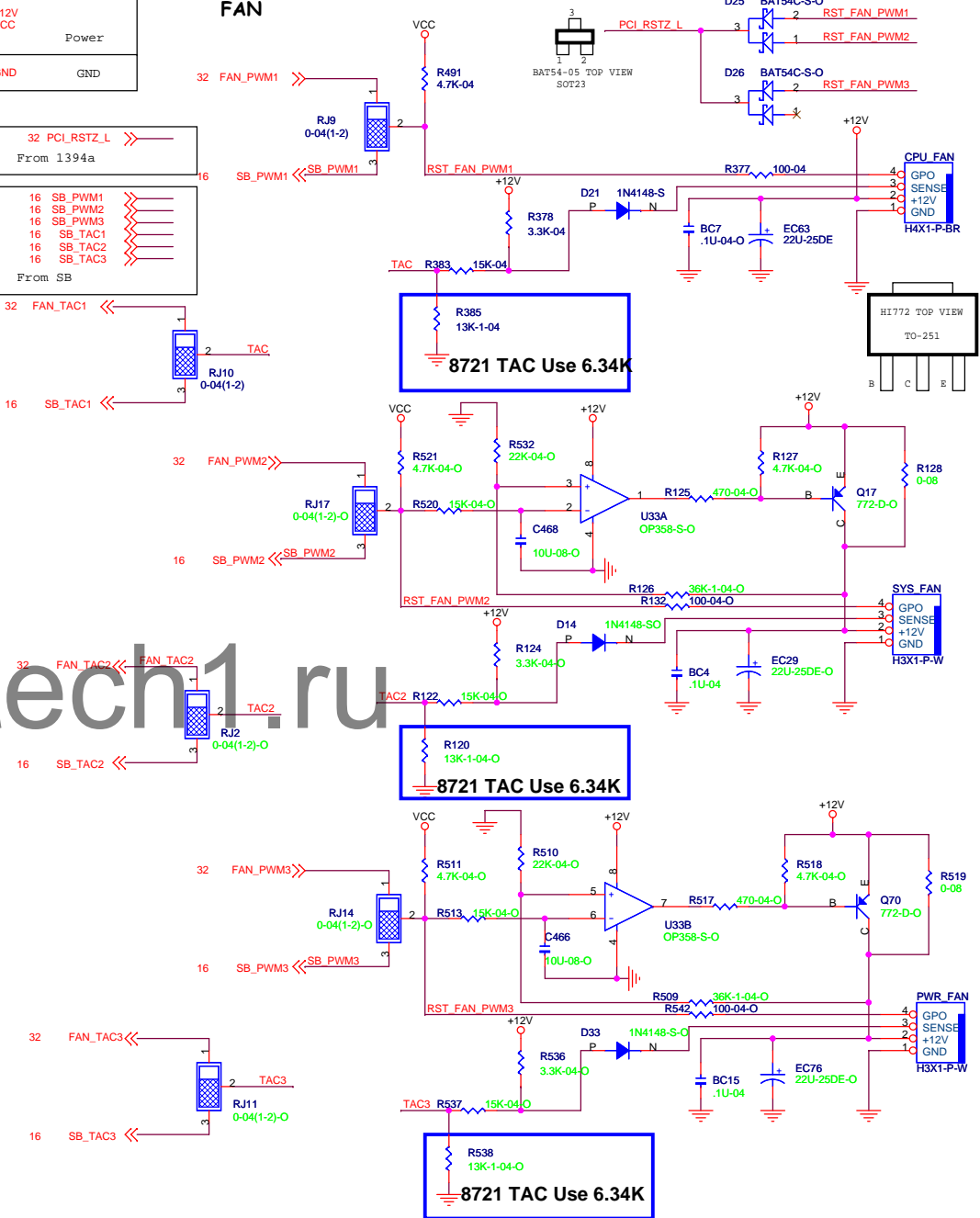
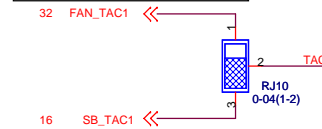
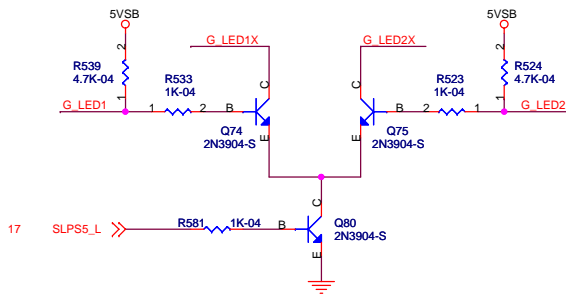
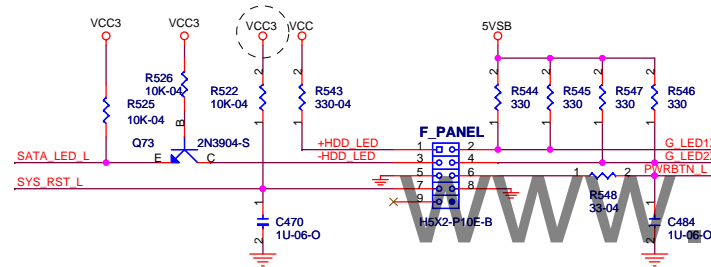
If without use pins 30,71,95, Please pull-up to VCC. Don't let it floating.

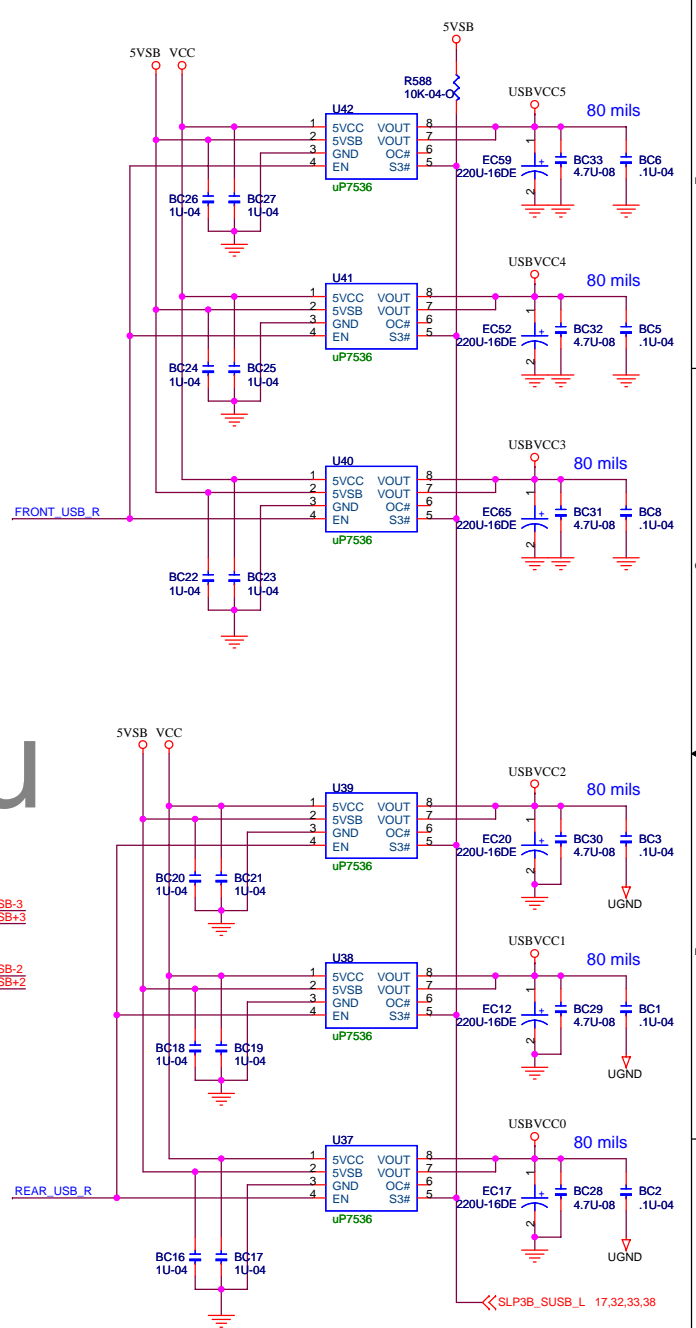
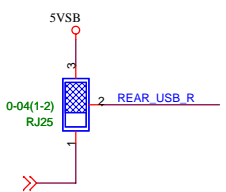
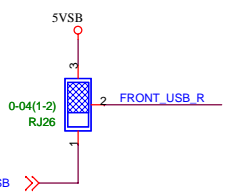
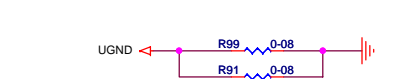
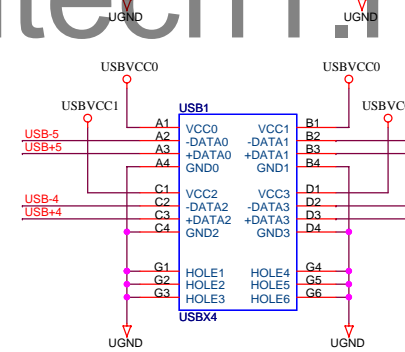
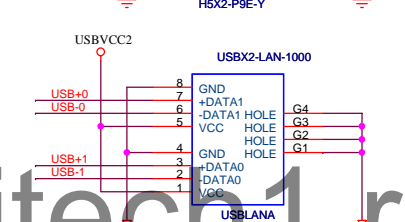
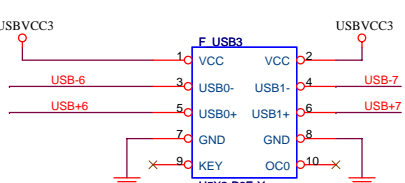
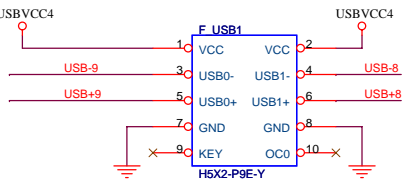
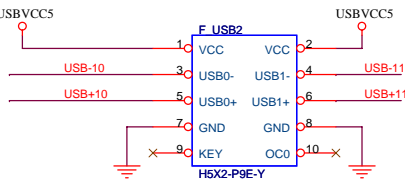
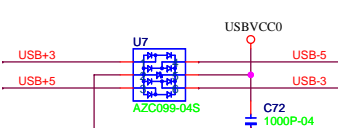
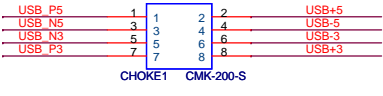
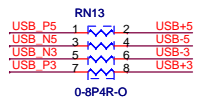
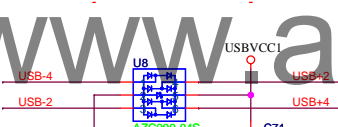
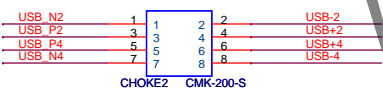
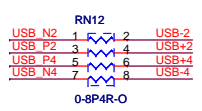
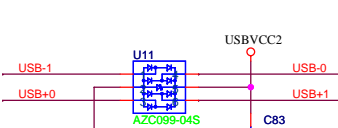
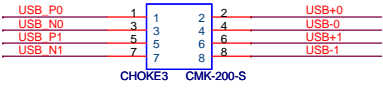
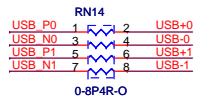
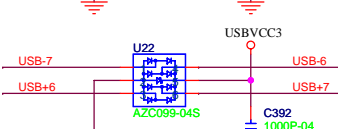
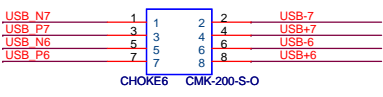
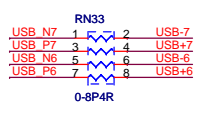
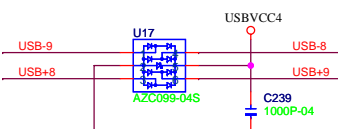
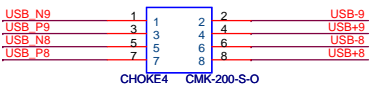
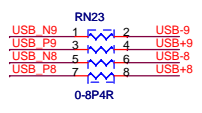
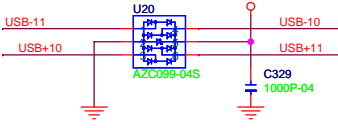
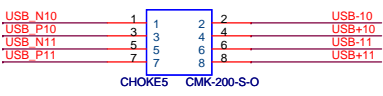
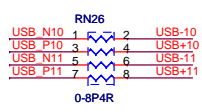
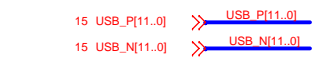


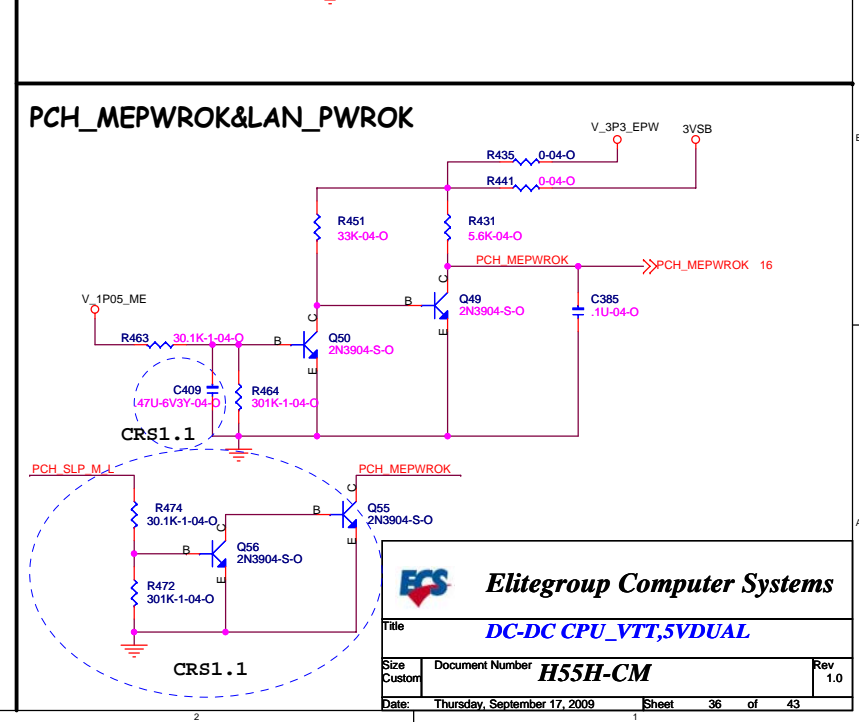
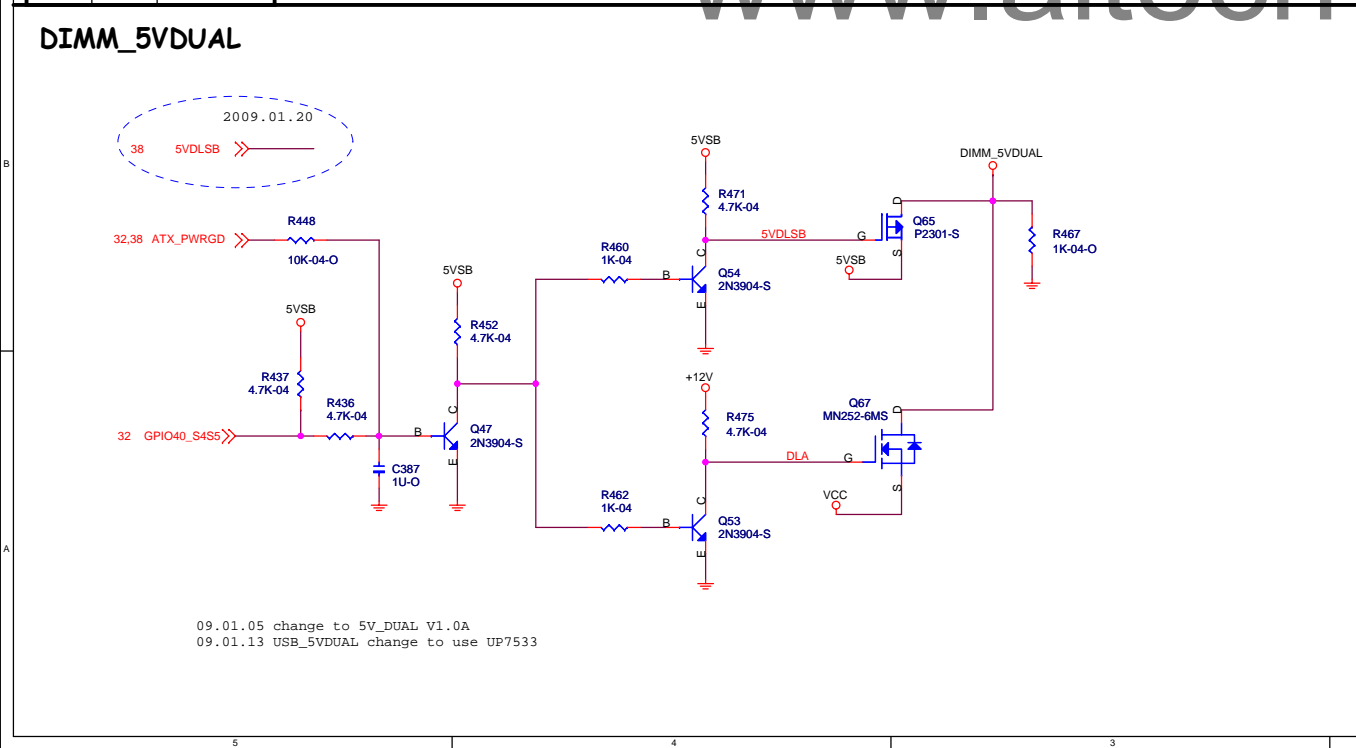
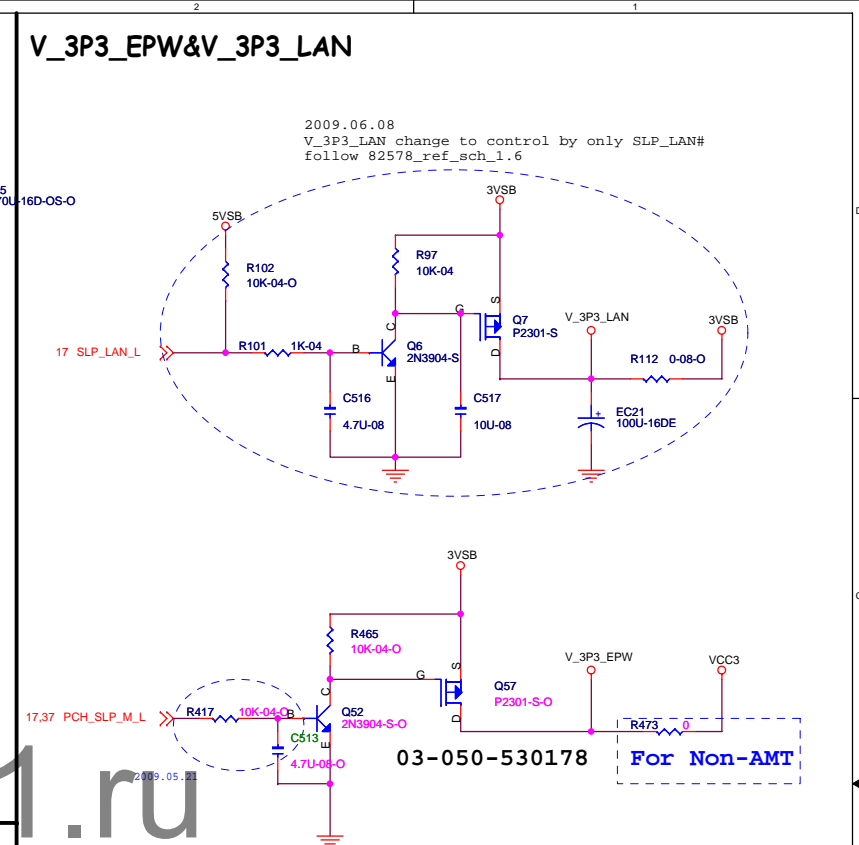
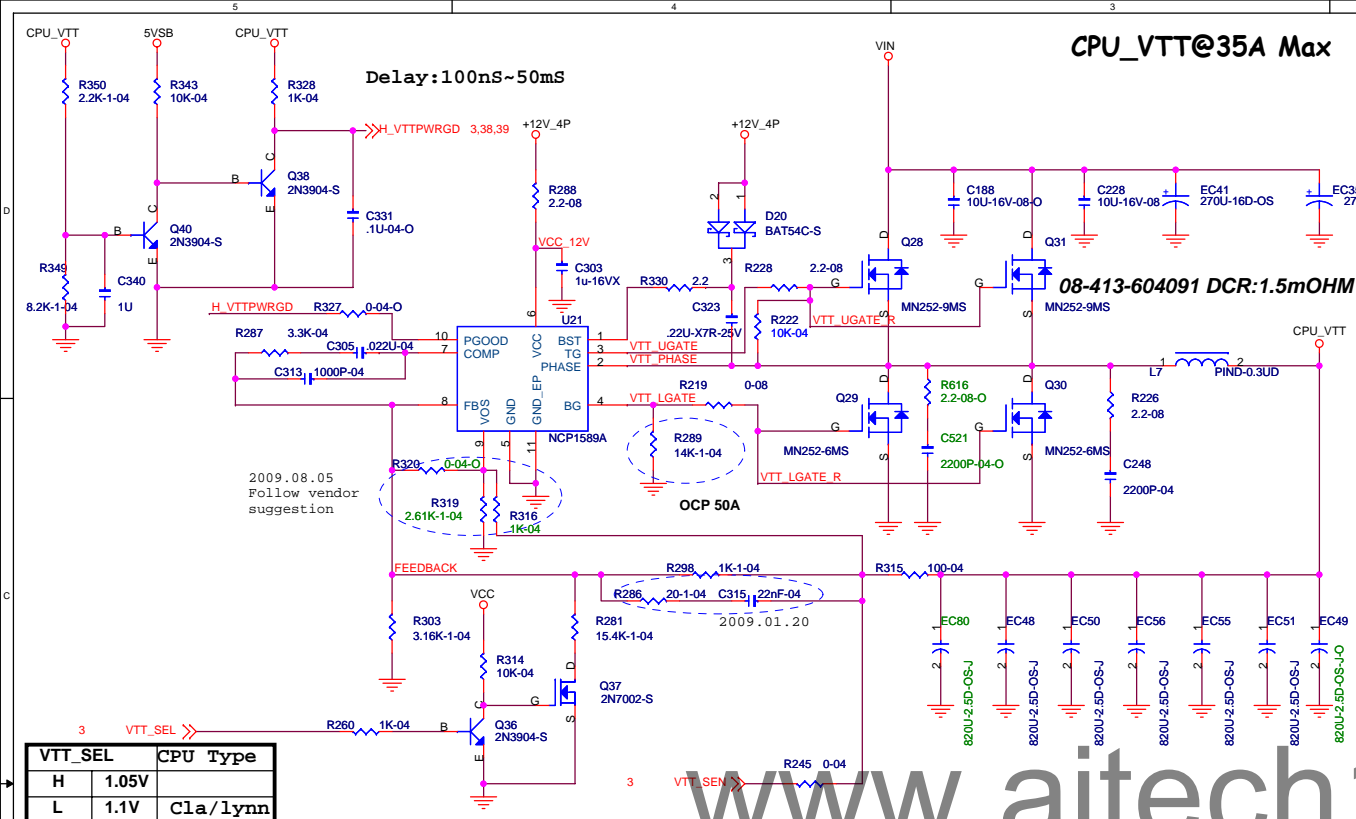


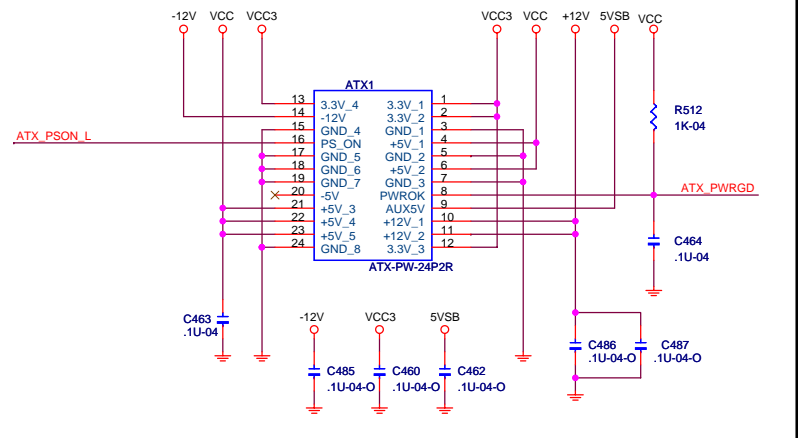
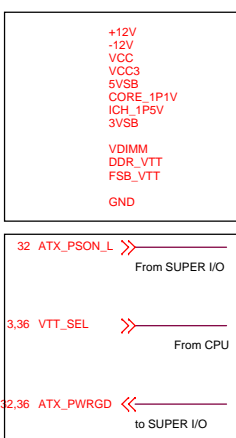


WW41 SYS_RST_L should
pull high to VCC3 not 3VSB

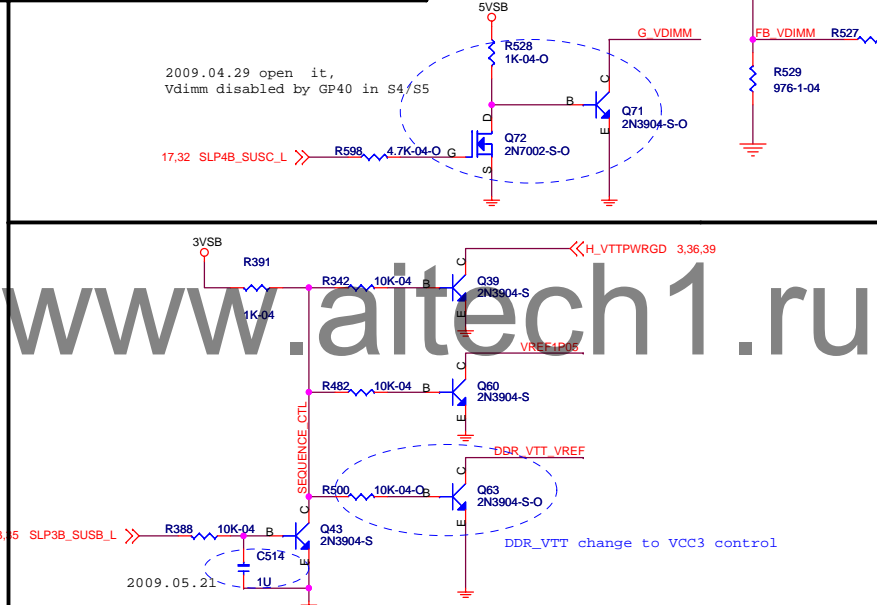
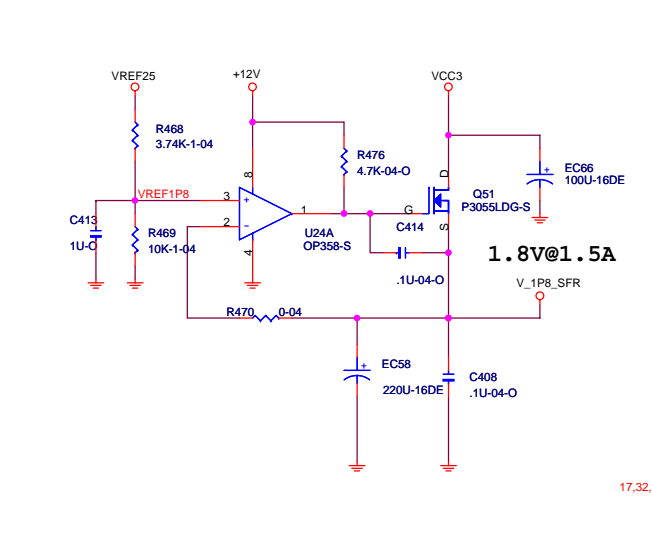




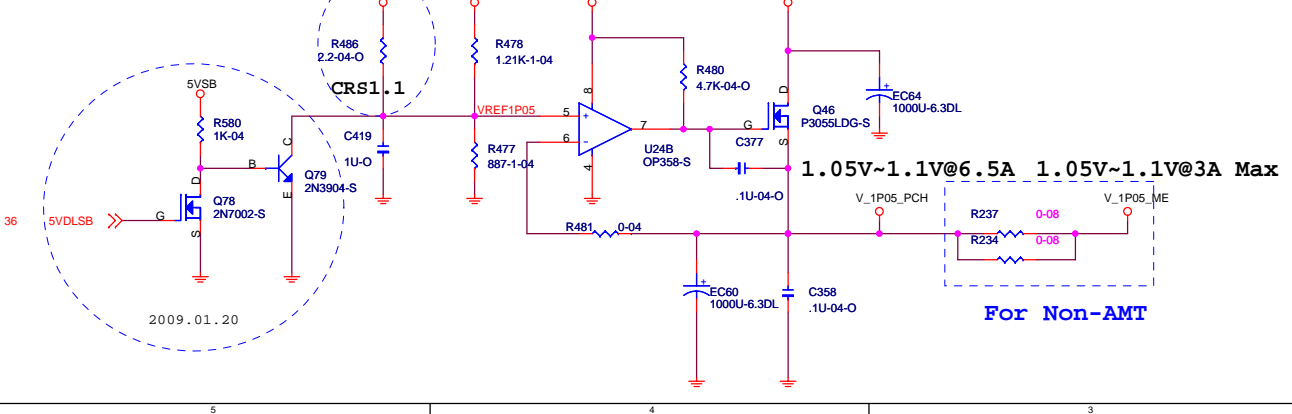




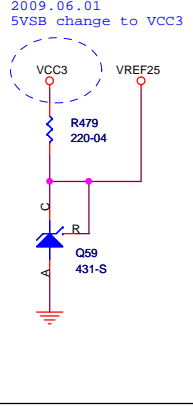
V_1P8_SFR



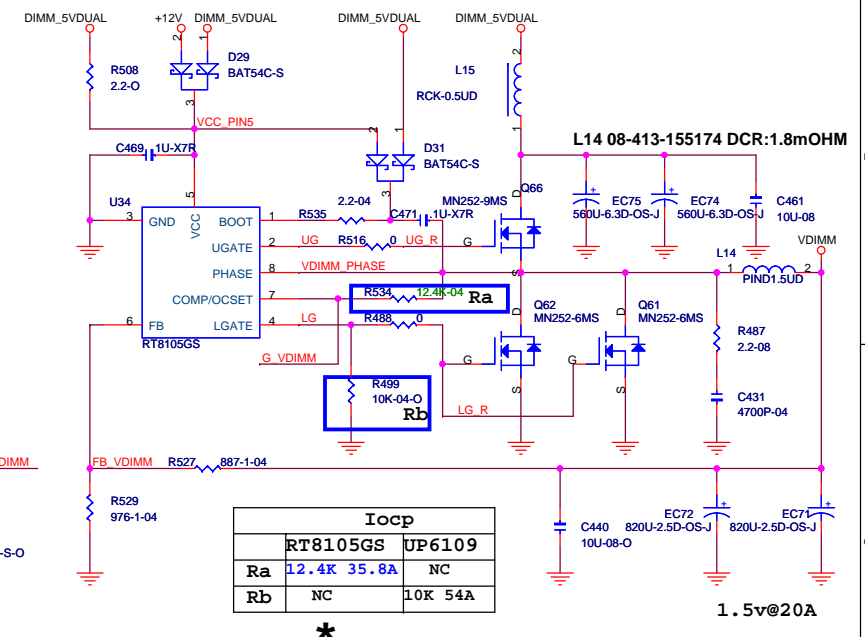
V_1P05_PCH



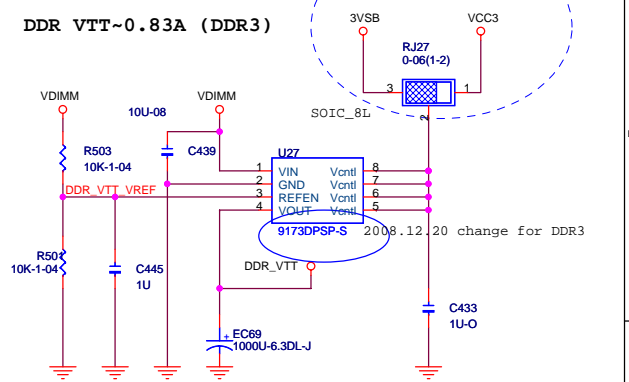
VREF25



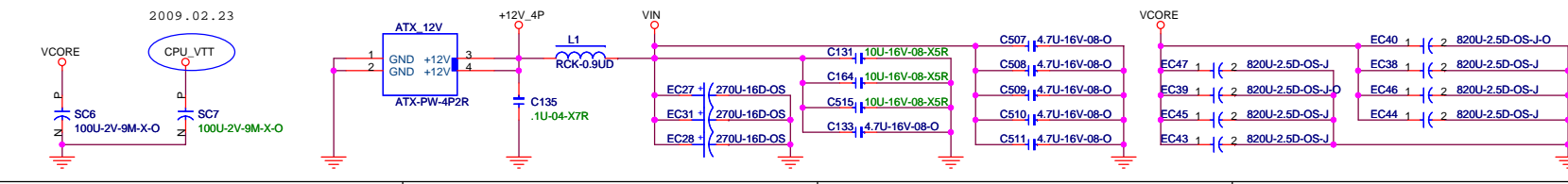
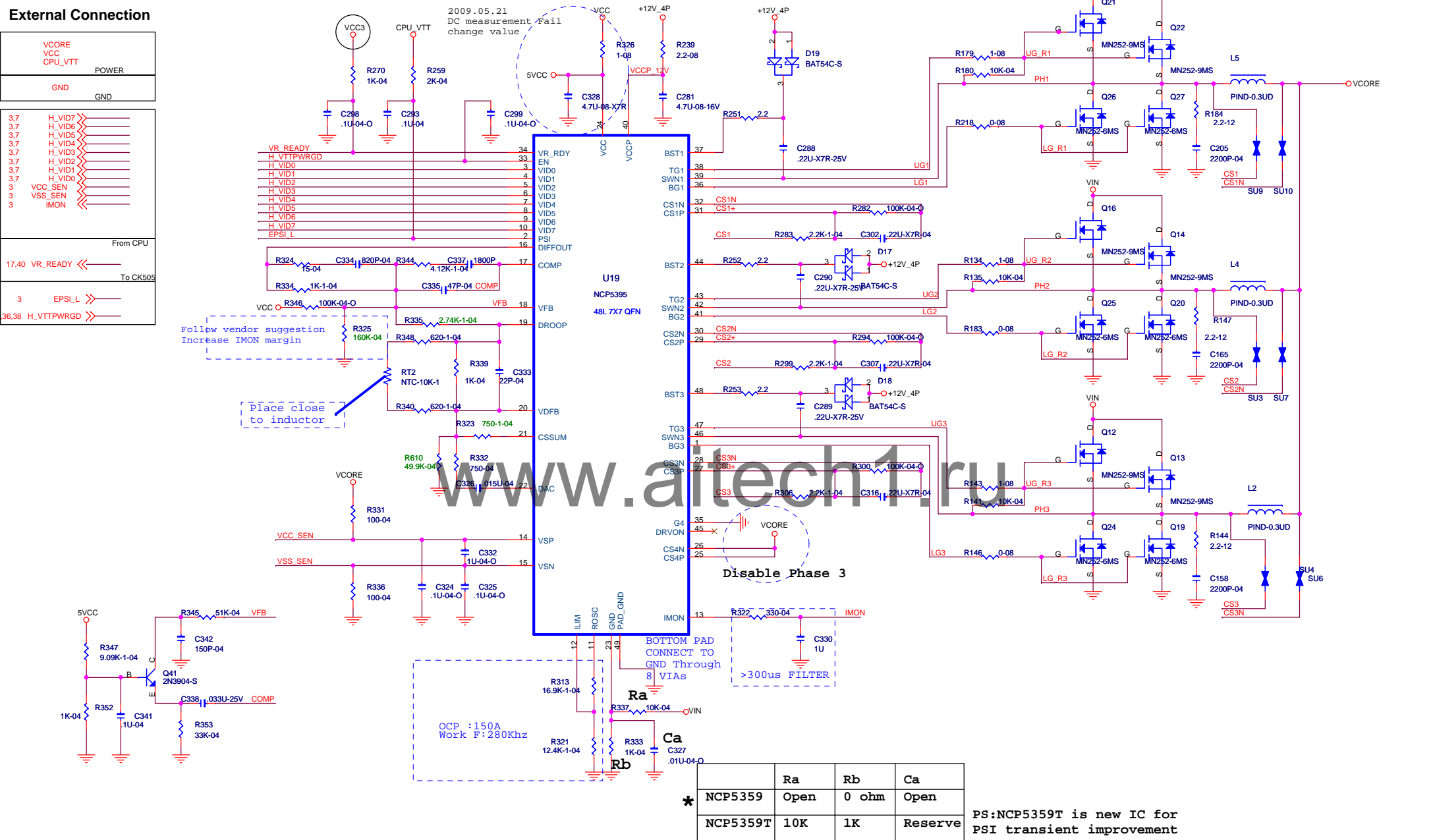
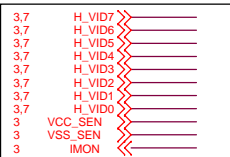
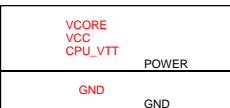
VDIMM



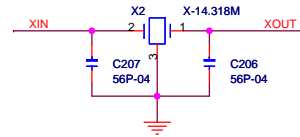
DDR_VTT



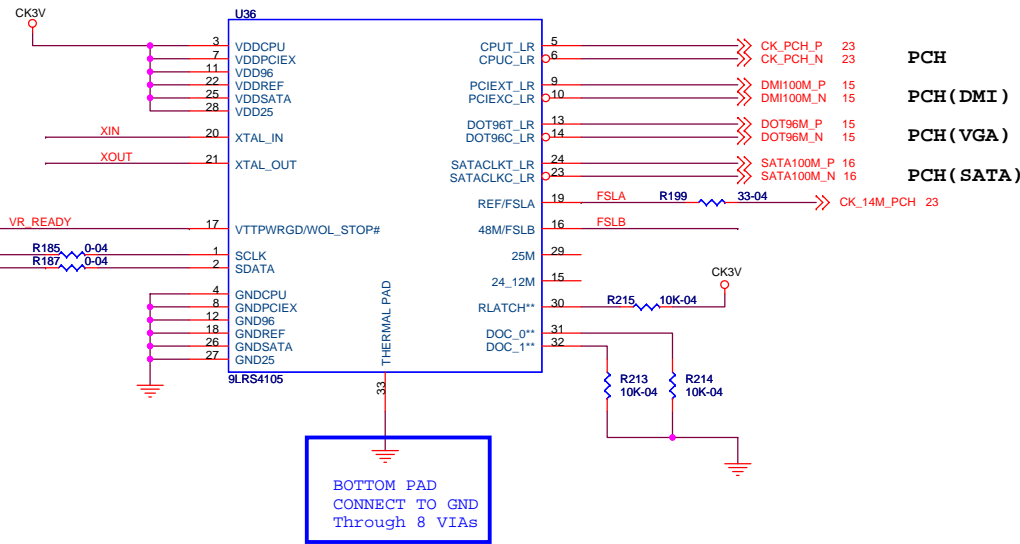
External Connection



The C206/C207 value depend on CL of X2 crystal
if CL=20pf C206/C207=33pf
if CL=32pf C206/C207=56pf

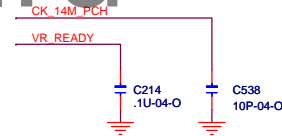
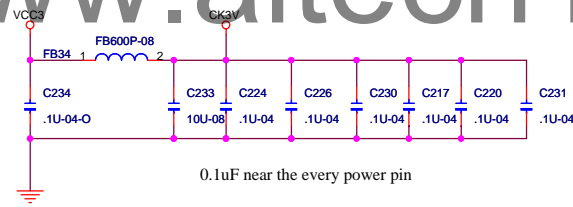
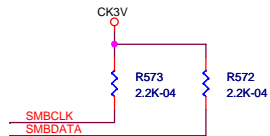


17,39 VR_READY >> VR_READY
10,11,12,13,14,17,19,24,27,28,32 SMBCLK >>>
10,11,12,13,14,17,19,24,27,28,32 SMBDATA >>>



FSLB, FSLA = 01, CPU_CLK = 133MHz

Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)
0	0	266.66
0	1	133.33
1	0	200.00
1	1	166.66



www.aitech1.ru

